FABRICATION AND CHARACTERIZATION OF ZnO-BASED THIN-FILM FIELD-EFFECT TRANSISTORS

By

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To my family for their love and encouragement.

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CHAPTER 1
INTRODUCTION

The principle of a field-effect transistor (FET) was first proposed in 1930. Since then, FETs have been studied intensively, and complementary metal-oxide-semiconductor (CMOS) integrated technology has progressed rapidly. The silicon industry expanded with CMOS technology because of its advantages: electrically stable Si-SiO_2 interface, high dielectric breakdown strength, and thermal stability at high temperature. The past decade in Si-based industry has seen Dynamic Random Access Memory (DRAM) manufacturing advance from low-scale-integration to the generation of Ultra-Large-Scale Integration (ULSI). In recent years there has been a shift from a technology generation strategy to a shrink strategy with shorter development cycles.

Field-effect transistors have also been investigated using III-V semiconductors, such as GaAs and GaN. The advantages of GaAs-based TFT over Si-based devices are high speed and high-power applications, in part from electron mobility in GaAs that is 5 times greater than that in Si, and a high breakdown field. GaN compound semiconductors also possess excellent properties that include wide band gap, high critical breakdown field, and high electron saturation velocity, which have encouraged the rapid development of GaN-based transistors over the past decade. However, the obstacle to GaAs or GaN-based MOSFET devices is the lack of high-quality, thermodynamically stable insulators on semiconductor for use as a gate dielectric that can match the device criteria of SiO_2 on Si.

The recent surge of interest in ZnO which is in the group III-V alloy system plays an important role in expanding the area of semiconductor technology. ZnO is particularly attractive in terms of low-temperature synthesis and a direct wide band gap. Because of its intrinsic defects, ZnO exhibits n-type semiconducting behavior at room temperature. Much recent effort was made to synthesize p-type ZnO to fabricate a field junction device for FET and light emitting diode (LED). Table 1-1 shows the properties of selected semiconductors at room temperature.

My study focused on fabrication and characterization of ZnO-based thin-film field-effect transistors. To understand the operation and enhance the performance of field-effect transistor, I studied gate oxides such as $CaHfO_x$ and $(Ce,Tb)MgAl_{11}O_x$ in the forms of metal-insulator-metal (MIM) and metal-insulator-semiconductor (MIS) structures.

Chapter 2 reviews the background of MOS technology. The theory of high-k dielectrics is revised and several gate oxides are introduced for the candidates of high-k dielectrics. In order to better understand the properties of the poly-crystalline ZnO transistors, the results of research for the poly-crystalline Si transistors are studied and recent results of ZnO FETs are introduced. Furthermore, the deposition methods of thin films are described. Chapter 3 gives the understanding of the crystallinity of $CaHfO_x$ on various substrates. The electrical properties of $CaHfO_x$ for the gate dielectric are explored in Chap. 4 in the form of MOS structure using Si substrate. Chapter 5 describes electrical properties of amorphous $(Ce,Tb)MgAl_{11}O_x$ thin films using ITO and Si substrates with MIM and MIS structures, respectively. Chapter 6 covers the depletion-mode field effect transistors with undoped ZnO and phosphorous-doped ZnO as an active channel. The structure of FET is introduced and electrical properties of devices using each channel material are discussed. Chapter 7 describes the enhancement-mode thin film transistor with phosphorous-doped (Zn,Mg)O as an channel layer. The device parameters are investigated from the electrical characteristics. Finally, my dissertation closes in Chapter 8 with the summary.

Table 1-1. Properties of selected semiconductors at room temperature

Properties	ZnO	Si	GaAs	GaN
Density (g/cm^3)	5.606	2.323	5.32	6.15
Stable phase (300K)	Wurtzite	Diamond	Zincblende	Wurtzite
Melting point (°C)	1975	1415	1238	>1700
Thermal conductivtiy (W/cm-°C)	0.6, 1-1.2	1.5	0.46	1.5
Static dielectric constant	8.656	11.9	13.1	9
Refractive index	2.008, 2.029	3.43	3.3	2.3
Energy gap (eV)	3.4 (Direct)	1.12(Indirect)	1.424(Direct)	3.4(Direct)
Intrinsic carrier density (/cm^3)	$< 10^6$	1.45×10^{10}	1.79×10^6	1.9×10^{-10}
Electron effective mass	0.24	0.98	0.067	0.19
Hole effective mass	0.59	0.16	0.082	0.6
Electron hall mobility (300K) (cm^2/V-s)	200 (Bulk)	1500	8500	1000(Bulk) 2000(2-D gas)
Hole hall mobility (300K)	25	450	400	30

CHAPTER 2
LITERATURE REVIEW

2.1 High-k Dielectrics

Since the beginning of integrated circuit production in the early 1960s, silicon dioxide, SiO_2, has been used primarily as a gate dielectric film in MOSFET structures. However, scaling metal-oxide-semiconductor field-effect transistor (MOSFET) channel length to submicron feature sizes requires a corresponding reduction in the gate dielectric thickness to achieve high performance. Circuit performance trends can be characterized by switching time, which results in rapidly shrinking transistor channel lengths and thinning gate dielectrics. The SIA Roadmap [1] in Table 2-1 shows the minimum feature size and equivalent gate oxide thickness of MOSFETs. The drain current in the saturation region is described by

$$I_D = \frac{W}{L}\mu C_{ox}\frac{(V_D)^2}{2}$$

where W is the width of the transistor channel, L is the channel length, μ is channel carrier mobility, and C_{ox} is the capacitance of gate dielectric. If carrier mobility is assumed to be constant, in order to increase I_D, either a reduction in channel length or an increase in capacitance of the dielectric is required. The capacitance of the dielectric is expressed as

$$C = \frac{\kappa\varepsilon_0 A}{t}$$

where κ is the dielectric constant, ε_0 is the permittivity of free space, A is the area of the capacitor, and t is the thickness of the dielectric. To increase capacitance, the dielectric constant should be high or the thickness of the dielectric should be thin. For SiO_2, the dielectric constant is 3.9, and the thickness can vary. However, below practical limits of thickness, SiO_2 has a large gate leakage current across the dielectric, due to direct tunneling. Thus new materials with higher permittivity than SiO_2 are needed to improve circuit performance. To achieve the same capacitance density of the dielectric with SiO_2, the actual physical thickness of an alternative dielectric can be described by

$$C_{1(SiO_2)} = C_{2(high-k)} = \frac{3.9\varepsilon_0 A}{t_{eq}} = \frac{\kappa_{high-k}\varepsilon_0 A}{t_{high-k}}$$

$$t_{high-k} = \frac{\kappa_{high-k}}{3.9} t_{eq}$$

In selecting a gate dielectric with a higher permittivity than that of SiO_2, band offset must be considered to prevent high leakage currents. Since many potential gate dielectrics have reported no band offset values, the closest, most readily attainable indicator of band offset is the bandgap of the dielectric. A large bandgap generally corresponds to a large band offset. Information on the several dielectrics in Figure 2-1 shows that the dielectric constant generally exhibits an inverse relationship to the bandgap. Because of this relationship between permittivity and bandgap, high permittivity dielectric is not necessary. A moderate dielectric constant and a high band offset are needed to produce a large tunneling barrier. The basic idea for using high-k materials is to increase film thickness to reduce the tunneling leakage current and improve reliability.

When thin film is gate dielectric on a silicon circuit, the interface between dielectric and silicon is also important. Generally, most high-k metal oxides are more unstable with silicon than with SiO_2, because of thermodynamic stability. They usually react with silicon to form an undesirable interface layer, which lowers overall capacitance and also sets a limit on the minimum achievable t_{eq}. The capacitance of two dielectrics in series is given by

$$\frac{1}{C_{tot}} = \frac{1}{C_1} + \frac{1}{C_2}$$

If the structure of the dielectric stack includes a SiO_2 bottom layer and a high-k alternative gate dielectric top layer, equivalent thickness can be described by

$$t_{eq} = t_{sio_2} + \left(\frac{3.9}{K_{high-k}} \right) t_{high-k}$$

where t_{eq} and $t_{high\text{-}k}$ are the equivalent oxide and physical thickness, respectively, and t_{SiO2} and $K_{high\text{-}k}$ are the thickness of silicon dioxide and dielectric constant of the other dielectric, respectively.

Interface traps are defects related to the chemical bonds located at the interface between semiconductor and insulator in MOS devices that introduce unwanted energy levels in semiconductor bandgap. Such defects are produced by a variety of mechanisms, including processing procedures, exposure to ionizing radiation, impurities, and hot carrier effects. Interface traps can significantly degrade the performance of MOS devices by exchanging charge with Si [2-4].

2.2 Electrical Transport in Dielectric Films

2.2.1 Introduction

Insulating films are required to electrically isolate conducting components or devices and to serve as the dielectric within capacitors. The traditional picture of an insulator is a material that possesses very few charge carriers at practical temperatures. This is a consequence of the large energy band gap. In practice, however, insulating films are generally amorphous, and the usual model of sharply defined energy bands cannot be readily applied. Because of its structural imperfections, there may actually be a relatively high density of charge carriers. They tend to be localized or trapped at these centers for long times, and the insulating behavior stemming from such carriers has very low mobility.

2.2.2 Fowler-Nordheim Tunneling

In case of thick insulator film, no detectable current flows until Fowler-Nordheim (F-N) emission due to field-assisted tunneling occurs at a large electric field above 6~7 MV/cm. When electric field is further increased beyond 10~12 MV/cm, depending on the film thickness and so on, dielectric breakdown occurs, as discussed in References [5-7]. Fowler-Nordheim current density J will lie on a straight line if $\ln(J/E_i^2)$ is plotted as a function of $1/E_i$, the slope of which will give the barrier height Φ_B. This conduction process has the strongest dependence on the applied voltage but is essentially independent of the temperature. When thickness is reduced to less than 4~5 nm, direct tunneling becomes dominant.

2.2.3 Direct Tunneling

Tunneling involves charge transport through an insulating medium separating two conductors that are extremely closely spaced. Electrical conduction in discontinuous metal films occurs by electron tunneling between islands when the interparticle spacing is small enough. At sufficient high values of electric field, electrons penetrate into the vacant insulator conduction-band states rather than surmount Φ_B vertically as in Schottky emission. Tunneling cannot occur classically but is rather a quantum mechanical effect. Because the metal wave functions extend into the insulator, there is a probability that electrons can exist there. If the insulator is thin enough, electron wave functions can even extend into the opposing metal [8]. A simple criterion that direct tunneling occurs rather than Fowler-Nordheim tunneling is given by

$$V_i \equiv E_i d < \Phi_B$$

Figure 2-2 shows conduction processes in ultra thin SiO_2 films as a function of electric field and thickness.

2.2.4 Schottky Emission

This conduction mechanism is very similar to thermionic emission of electron from a heated metal into vacuum [9-11]. Thermionic emission is described by

$$J_{TE} = AT^2 \exp(-q\Phi_M / kT)$$

where Φ_M is the work function and A is the Rechardson constant equal to 120 $A/cm^2\text{-}K^2$. Typically, $q\Phi_M$ is equal to 4~5 eV. Rather than acquire energy, electron need only surmount the smaller energy barrier $q\Phi_M$ to access the empty conduction-band states of the insulator. Values of Φ_M depend on the particular metal-insulator or metal-semiconductor contact. The origin of Schottky effect in high electric fields is due to the continuously varying rather than abrupt electron potential energy distribution at the metal-insulator junction. When the electron enters the insulator, charge is redistributed on the electrode to maintain equi-potential surfaces. The result is to produce a so-called image field that adds to the applied field and helps to round and lower the potential barrier.

2.2.5 Poole-Frenkel Emission

Bulk charge trapped by impurity levels in the insulator band gap can be transferred to the conduction band by internal emission processes. In Poole-Frenkel emission the impurity is viewed as an ionized donor with a hydrogen-like Coulomb potential. When filled by an electron, the defect center is neutral. In an applied field the potential well distorts asymmetrically. Trapped electrons can escape by thermal activation over the reduced energy barrier corresponding to that required to ionized donor. Net current flows due to successive electron jumps between Poole-Frenkel traps. The factor of 2 difference between Poole-Frenkel and Schottky emission arises due to consideration of a fixed rather than image charge. A variant of Poole-Frenkel emission involves quantum mechanical tunneling into the insulator conduction band by electrons trapped within the spherical donor potential well [12-14].

2.2.6 Ionic Conduction

High temperature conduction in thick- film and bulk insulators frequently occurs by ionic rather than electronic motion. Ions are large cumbersome carriers of low mobility. They require high activation energies to execute nearest-neighbor diffusive jumps, and when ions diffuse thy also transport charge. Since ionic transport is basically solid-state electrolysis, atomic or molecular species will necessarily be discharged at the contacts.

An important example of ionic conduction is the migration of sodium ions in thin SiO_2 films. This phenomenon leads to operating instabilities in field-effect transistors [8].

2.3 Thin-Film Transistors Using Polycrystalline Semiconductor

2.3.1 Polycrystalline Silicon Thin-Film Field-Effect Transistors

Polycrystalline silicon thin-film transistors (poly Si TFTs) have been extensively studied due to their potential applications in high-performance active matrix liquid-crystal displays (LCD) on glass substrates [15]. Poly Si TFTs have a high field-effect mobility compared with amorphous silicon TFTs. Another advantage is their lower fabrication cost since hard glass substrates are used. In order to get further enhancement of the device performance, fabrication should be carried out under a low-temperature process, below 600°C, to prevent the substrates from shrinking.

However, the mobility in Poly Si TFTs is lower than that in the single crystal silicon because of their grain boundaries. The grain size of poly Si is usually on the order of 0.1~0.2μm [16] and recently, the maximum grain size of poly Si has reached 0.5μm [17]. Therefore, several grains would be present between the source and the drain in the channel of FET devices. Electron are scattered at the grain boundaries or are trapped by the interface states, and device performance is degraded. Another role of grain boundary trap in poly-Si film is to increase threshold voltages [18]. At high drain biases, the kink effect, the lack of saturation in the output characteristics, in the output characteristics is much more pronounced in poly-silicon TFTs compared to single-crystal devices [19-21].

The influence of the grain boundaries on the TFT performance has been investigated by considering the traps either localized at the grain boundaries and/or uniformly distributed throughout the materials. Thus, they can be divided into two types in the light of dimensional approaches, that is, one-dimensional and two-dimensional models. The former is the model that assumes uniformly distributed defects in the channel like for an amorphous-silicon TFT, and the latter is the model in which defects exist only at grain boundaries. The one-dimensional approach is available approximately only for the poly-silicon TFTs with small grains and large defects. The two-dimensional one is necessary because intrinsic properties of the poly-silicon TFTs with large grains and small defect densities are mainly affected by the grain boundary defects in general [22].

There are two electrical transport mechanisms in poly-silicon films, thermionic-emission (TE) limited [23,24] and drift-diffusion (DD) limited [25]. Grain boundary trapping models based on the TE transport explained successfully the mobility dip and related resistivity problems of doped poly-silicon films. Thermionic emission theory is assumed that the barrier height is sufficiently larger than kT/q. In this model, the grain boundaries are considered as two-dimensional interfaces or defect-concentrated layers. On the other hand, a DD approach was also proposed to explain them and the temperature dependence of resistivity. In this model, the grain boundaries are considered as amorphous layers with a finite thickness. The DD conduction in grains and hopping transport in the grain boundary layers are assumed. DD conduction is likely to be more adaptable for undoped poly-silicon films because of the nonexistence of potential barriers and no emitted charges at the grain boundaries. Simeonov et al. [26] considered both TE conduction at the grain boundaries and DD conduction across the space-charge regions around the grain boundaries. This combined process was synthesized to describe the transport process across the grain boundaries in doped semiconductor films. Then the current is not necessarily under either TE or DD limit.

Figure 2-3 shows the energy band along the n-channel of poly-silicon TFT [20]. To determine the potential profiles along the channel in the defect-free crystallite regions and in the grain boundary regions, the Poisson's equations are used

$$\frac{\partial^2 V}{\partial x^2} = -\frac{q(n-p-N_d^+)}{\varepsilon_s}$$

and

$$\frac{\partial^2 V}{\partial x^2} = \frac{q(n-p-N_d^+)}{\varepsilon_s} + \frac{qn_t}{\varepsilon_s}$$

respectively, where n, p, N_d^+, and $n_t = n_a - n_d$ are the electron density, the hole density, the ionized shallow donor density, and the net negative charge in the grain boundary, respectively. And n_a and n_d are the occupied acceptor-like trap density and unoccupied donor-like trap state density in the grain boundary, respectively. This net negative charge n_t depletes neighboring electrons of grain boundary and causes exposure of the ionized shallow donors N_d^+, which in turn results in a band bending around the grain boundary. Consequently, a double Schottky barrier is formed at electrostatic and thermal equilibrium. This double Schottky barrier is the main obstacle for the carriers to transport through the poly-silicon channel [27].

For bias applied along the channel, the schematic energy band of poly-silicon TFT is shown in Figure 2-4 [21]. When the grain boundary depletion width W_{gb} is smaller than the grain size L_{grain}, the voltage drop V_a in one grain is divided into V_{gb} (grain boundary region) and V_c (inside the grain).

Several methods have been proposed to determine the density of states (DOS) in poly-silicon films. The most common approach is based on the analysis of the field-effect conductance (FEC) and Levinson's method. King et al. [16] determined the midgap-state density of poly-silicon with these two methods.

The FEC-analysis method assumes that defects within a poly-silicon film are uniformly distributed throughout the materials, and that the corresponding density of states in the poly-silicon band gap is continuous in energy. In contrast, Levinson's method assumes that defects are localized at grain boundaries and correspond to monoenergetic trap states in the poly-silicon band gap, so that the trap-state density is proportional to the square root of the slope in the plot of $\ln(I_{DS}/V_G)$ vs $1/V_G$ at a low drain bias (0.1V). The grain boundary trap model has been employed to monitor the reduction in apparent trap-state density during hydrogenation. Levinson's model may only be appropriate for large-grain, low-defect-density film. Therefore, FEC method provides a more sensitive measure of trap-state-density reduction that Levinson's method.

Much work has focused on determination of density of states in the poly-silicon using conductance method because the characteristics of poly-silicon devices are strongly dependent on the density of states distribution in the forbidden gap. Figure 2-5 shows the density of states obtained by using n-channel and p-channel transistors for energies above and below E_{F0}, respectively. E_{F0} is the Fermi energy in flatband conditions. Fortunato et al. [28] showed the exponential tail slope of the density of states near the conduction band edge in the poly-silicon FETs. Tail states arise from distorted-bond defects, whereas deep trap states located near the mid gap arise from dangling-bond defects [22,29,30].

From this reason, deep trap state is reduced by hydrogenation, but the band tail is expected to exist in hydrogenated films as well [31].

It is generally agreed that the conductance of poly-silicon TFTs is dominated by grain boundary potential barriers. The conductance, $G = (I_{SD}/V_D)(L/W)$, is thermally activated and is described by the expression.

$$G = G_0 \exp(-E_a/kT)$$

where L/W is the channel length/width ratio and k, and T stand for the Boltzmann constant, and the temperature, respectively. The field effect activation energy E_a and the conductance prefactor G_0 are determined at each gate voltage from the Arrhenius plots of lnG vs 1000/T. The activation energy E_a is the energy difference between the conduction-band edge E_C and the Fermi level E_f for n-channel TFTs. The field effect activation energy is a function of gate voltage, V_G, because of the different band bending conditions at increasing values of V_G. Dimitriadis et al. [29,32] showed the relations between activation energy and gate voltage, indicating that activation energy decreased slowly with gate voltage. From the Meyer-Neldel (MN) rule [33] that the conductance prefactor G_0 increases exponentially with E_a, the conductance prefactor is expressed as

$$G_0 = G_{00} \exp(AE_a)$$

where A is the MN parameter and G_{00} is conductance constant. From the plot G_0 vs E_a, G_0 increases exponentially with E_a, indicating that barrier height V_b is temperature dependent. With a MN parameter extracted from the slopes of the straight line, the barrier height can be expressed as

$$qV_b = Ea - AkTE_a$$

Therefore, the grain boundary height can be obtained as a function of gate voltage.

Figure 2-6 [34] shows that the potential barrier height increases with increasing the gate bias at first, reaches a peak value at the onset of strong inversion, and then decreases. Since some induced carriers are captured by the traps, the barrier height increases initially with increasing gate bias. As the gate bias is further increased, all of the traps are filled, and the total trapped charges remain the same. But, the lateral depletion width decreases, the barrier height rolls off. Moreover, if the grain size is small, the barrier height will be low due to the fact that surface band-bending at the onset of strong inversion decreases with decreasing grain size.

The formation of a potential barrier in the polycrystalline Si substrate channel is due to the fact that carriers are trapped at the localized grain-boundary states, and in turn, these trapped charges deplete free carriers near the grain boundaries. For a p-type poly-silicon substrate, holes are trapped at the grain boundaries. When a positive voltage with respect to the substrate is applied to the gate, the energy band is bent down toward the Si-SiO_2 interface. The traps distributed in the regions where the trap level moves closer to the Fermi levels are gradually filled by induced electron. Thus, some of the total electric-flux lines emanating from the gate are terminated by the trapped charges in the grain boundaries. From this reason, the smaller grain size is, the larger the threshold voltage will be [33].

Poly-silicon device exhibit the kink effect in their output characteristics at high drain biases that is undesirable in circuits of analog applications. It was reported that this effect was caused by the avalanche generation mechanism, grain boundaries, or traps in the poly-silicon. Dimitriadis et al. [19] investigated the influence of the channel length and the grain size on the kink effect in low pressure chemical vapor deposited (LPCVD) poly-silicon. Their results indicated that kink effect is more pronounced in the short channel device because avalanche multiplication causes kink effect in the output characteristics due to the high electric fields at the drain junction. With a short channel device, they changed deposition pressure and investigated the grain size effects. The kink effect was more pronounced with decreasing the deposition pressure or increasing the grain size of poly-silicon. It is well known that electrical performance of device is degraded by the presence of carrier traps at the grain boundaries. Even if the trap density was calculated from the Levinson's analysis, it was realized that the degradation in the output characteristics of poly-silicon TFTs couldn't be attributed only to the presence of carrier traps at the grain boundaries. It was concluded that the kink effect enhancement is due to high electric fields at the drain end caused by the enhanced lateral carrier diffusion from the source/drain contacts along the drain boundaries.

Another characteristics in the poly-silicon TFTs is high off-state current [31,35]. When negative gate voltage (V_G) is applied to an n-channel TFT, drain current (I_D) increases with $|V_G|$. This current is an off-state current in poly-silicon TFTs. Even if field emission, thermoionic field emission, or a generation of carriers at the drain junction can be predominant candidates as the off-state current mechanism, off-state current is not determined by an unique one because it is dependent on bias voltage, TFT size, or fabrication conditions. In the case of hydrogen-unpassivated TFTs, the I_D-V_G curves have a V shape while the I_D-V_G curves with hydrogen-passivated TFTs have a flat-bottomed trough shape.

2.3.2 Polycrystalline ZnO Thin-Film Field-Effect Transistors

In recent years, metal-oxide semiconductor films have been widely studied and have received considerable attention. Some of them are good candidates for transparent conductive oxides (TCOs) if they are prepared off-stoichiometry or doped with a suitable impurity [36]. Among TCOs, ZnO oxide (ZnO) has many interesting characteristics. It is a II-VI semiconductor with a wide direct band gap of 3.37 eV at room temperature. If its semiconductor characteristics can be utilized, it is expected that light-emitting diode (LED) operating in the short-wavelength range, from blue to ultraviolet, and high power electronic devices could be realized with ZnO.

ZnO is one of a few oxides that can be grown as a crystalline material at relatively low deposition temperatures on various substrates such as amorphous glasses. Due to these characteristics, Several TFTs of relevance to the work have been reported recently. Hoffman et al. [37] reported bottom-gate-type thin film transistor was fabricated using undoped ZnO as an active channel deposited via ion beam sputtering. Semiconducting oxide layer was grown at room temperature and a rapid thermal anneal (RTA) was employed to consider channel resistivity, interface between gate oxide and channel layer, and crystallinity of ZnO layer. Their device operated as an n-channel enhancement-mode TFT and its effective channel mobility and threshold voltages were found to be 0.35-0.45 cm^2/V s and 10-15 V, respectively. Masuda et al. [38] also reported bottom-gate ZnO-TFT using pulsed laser deposition at 450°C. They fabricated three kinds of devices with undoped ZnO for an active channel layer. The first one had a two-layer gate insulator of SiO_2 and SiN_x and a gate of heavily doped p-type crystalline silicon. The device showed enhancement-mode operation, and had the I_{on}/I_{off} ratio of 10^5. The field effect mobility and the threshold voltage were 0.031 cm^2/V s and 2.5 V, respectively. The second device also had the double-layer gate insulator. However high carrier concentration ZnO was used for channel layer showing depletion-mode operation and two order of I_{on}/I_{off} ratio. Its field effect mobility and the threshold voltage were 0.7 cm^2/V s and -1 V, respectively. The last device fabricated using the gate of ITO and the substrate of glass showed depletion-mode operation. Another transparent ZnO thin-film transistor was reported by Carcia et al. [39]. The bottom-gate ZnO-TFT with channel length of 20μm was fabricated at room temperature using rf sputtering. They used undoped ZnO for an active channel layer and SiO_2 for a gate oxide. Their device operated as an n-channel enhancement-mode TFT and field effect channel mobility was found to be 1.2 cm^2/V s.

Hossain et al. [27] modeled the grain boundaries in ZnO TFTs and performed simulation of a ZnO TFT by using a two-dimensional device simulator in order to determine the grain boundary effects on device performance. They approached polycrystalline ZnO TFT modeling with a single grain boundary in the middle of the TFT channel, in which a double Schottky barrier was formed in the grain boundaries, and its barrier height was analyzed as a function of defect density and gate bias. Developed potential barrier is expressed as

$$V_b = qN_t^2 / 8\varepsilon_s n$$

where V_b is the potential barrier, n is the free carrier concentration at thermal equilibrium in the crystallite regions, ε_s is the permittivity of ZnO, and N_t is the total trap state density. The effect of grain boundaries on TFT properties was investigated by calculating how the potential barrier V_b changes in the grain boundaries upon applying gate voltage V_g. As gate voltage increases, the carriers are accumulated at ZnO and gate oxide interface, and potential barrier decreases rapidly, whereas, at the locations far from interface, potential barrier decreases slowly and becomes independent of gate oxide. This is due to the fact that the effective field developed by gate bias does not propagate deeply into the channel. The simulation was extended to TFTs with many grain boundaries to quantitatively analyze the potential profiles that developed along the channel. Unlike polycrystalline silicon TFTs with large grain size, polycrystalline ZnO TFTs have nano-scale grain due to low temperature deposition and therefore, the each grain boundary is closed. Grain boundary depletion region are overlapped to lift the minimum conduction band edge up from the equilibrium Fermi level resulting in the activation energy higher than the qV_n. Consequently the concentration of thermally activated carriers becomes smaller, and more exposure of ionized donor makes the film semi-insulating. Further reduction of grain size results in lifting up the conduction band edge further away from the Fermi energy level, and the depletion region overlaps to spread over the entire film, leading to very high film resistivity with large thermal activation energy. If the situation occurs for a particular small-grain thin-film without applying any gate bias, then the positive gate bias is required to enhance carriers for operating a TFT. This operational mode of TFT is known as enhancement-mode of operation. Through this simulation, they estimated the density of total trap states localized in the grain boundaries for polycrystalline ZnO TFT.

2.4. Growth Techniques

2.4.1 Pulsed Laser Deposition (PLD)

2.4.1.1 The PLD system

Pulsed laser deposition is conceptually and experimentally a relatively simple technique. A simplified schematic with the main features of the PLD method is shown in figure 2-7. The main components include a pulsed excimer laser beam with the ultraviolet wavelength range (193 or 248 nm)[40]. The laser beam is directed at a target located in a vacuum chamber in such a way that it generally impacts on the target surface at a 45° angle of incidence. The laser beam passes through both a quartz suprasil lens and window before entering the deposition chamber. The lens and window material is chosen so that there is a minimum absorption of laser light and therefore maximum attainable laser energy deposited on the target. The impact of the laser beam on the target surface results in various complicated processes including ablation, melting, and evaporation of material, and production of a plasma due to excitation and ionization of the species transformation of electromagnetic energy into electronic excitation, followed by a conversion into thermal, chemical, and mechanical energy. The materials ejected form the target is deposited on a substrate generally positioned opposite the first, as indicated in figure 2-7.

2.4.1.2 Overview of fundamental laser-solid interaction processes

Processes occurring during the interaction of a laser beam with a solid are is not so simple, with a large number of variables affecting the properties of the film, such as laser fluence, background gas pressure and substrate temperature. However, several models have been proposed during the past years, which have served as the basis for researchers to acquire a better understanding of the basic phenomena involved in laser-solid interaction.

The general view is that materials removal from a solid impacted by a laser beam involves a two-step process. As the laser beam hits the target surface, photons are absorbed and their energy is coupled into the materials, which results in the formation of a molten layer that vaporizes. The vaporization process creates a recoil pressure on the liquid layer, which contributes to expel the molten material. Thus, the material removed is a combination of vapor and liquid.

Efforts to understand the laser beam-solid interaction during the deposition of multicomponent oxide films have been largely related to HTSC materials and have concentrated mainly on characterizing the laser-generated plume. However, correlations between film quality and plume diagnostics have been made frequently. Current modeling of PLD builds on earlier laser-target work and includes a secondary interaction between the laser and the evaporated material. The interaction of a short-pulse, high-power (10^7-10^8 W/cm^2) laser with a ceramic target, under conditions appropriate for the growth of high-quality multicomponent oxide thin films, can be viewed as occurring in several stages in Figure 2-8 [41]. Optical irradiation of the target causes surface heating. The increase in the surface temperature depends on the optical penetration depth of the material, the thermal diffusivity of the target, and the rate at which energy is deposited into the system (laser pulse width). For metallic and small-bandgap materials the thermal diffusion distance is long compared to the optical absorption distance. Generally, the electronic structure (i.e. electronic states or bandgap) of the target is not important since the high electric fields generated by the laser result in dielectric breakdown (i.e. at these power densities all materials absorb a significant fraction of the radiation, resulting in surface heating). Under these conditions the surface temperature can exceed the melting temperature of a ceramic material (e.g., T_m (YBCO) $\approx$1400°C)

2.4.2 DC Magnetron Sputtering

Sputtering is one of the most commonly used methods for the deposition of thin films. Its popularity stems from the simplicity of the physical processes involved, versatility of the technique, and flexibility for alteration and customization. It is widely used in the semiconductor, photovoltaic, recording and automotive industries. In addition, specialized applications of sputtering in the manufacturing of sensors. Decorative glasses, optical devices, etc, are also very common. High melting point materials like ceramics and refractory metals which are hard to deposit by evaporative techniques are easily deposited using sputtering. Sputtering techniques range from a simple de glow discharge sputtering which is limited to the sputtering of conductive targets, to rf sputtering where any target regardless of its conductivity can be sputtered. In terms of deposition rates, there are sputtering techniques now available which rival evaporation or other higher deposition rate techniques deposition rates as high as 3 mg $cm^{-2}hr^{-1}$ have been reported by dual magnetron sputtering.

DC glow discharge sputtering is one of the simplest sputtering techniques. The limitation, as mentioned earlier, is that non-conductive targets cannot be sputtered by this technique. This is also not suitable for reactive puttering, especially where poisoning of the target may occur causing the formation of an insulating layer at the target surface. The only way an insulator target can be sputtered with a dc bias is by the use of a rotatable dc magnetron. Figure 2-9 shows a dc glow discharge sputtering system. The target, in the form of a plate, is made up of the material be deposited and is connected to a dc power supply capable of supplying several kilovolts the substrates face the target. Depending on the kind of film desired, the substrates can be water cooled or heated to a specific temperature. Electrically, the substrates could be grounded, biased or left floating. After pumping down to the base pressure and backfilling with the puttering gas, generally Ar, a negative voltage is applied to the target to tart the plasma. The positive ions in the plasma bombard the target surface and eject mostly neutral atoms of the target which are then condensed onto the substrate to form a film.

When a dc power is applied to the target, initially a very small current flows through the system due to a limited number of charge carriers in the system. As the applied target voltage increases, more and more charge carriers are created partly due to the secondary electrons that are emitted from the target and partly from impact ionization. As a result, the current rises and a 'Townsend discharge' is created. This is the beginning of an avalanche which leads to a steady state where the number of electrons and ions produced becomes the same and the plasma becomes self-sustaining. This is the normal glow state. The gas glow becomes increasingly visible accompanied by a sharp rise in the current and a drop in the voltage. This is the 'abnormal glow' state and also the normal sputtering regime.

Table 2-1. International technology roadmap for semiconductors (1999)

Production year	Minimum feature size (um)	Equivalent dielectric thickness (A)
1997	0.25	40 – 50
1999	0.18	30 – 40
2001	0.15	20 – 30
2003	0.13	20 – 30
2006	0.10	15 – 20
2009	0.07	< 15
2012	0.05	< 10

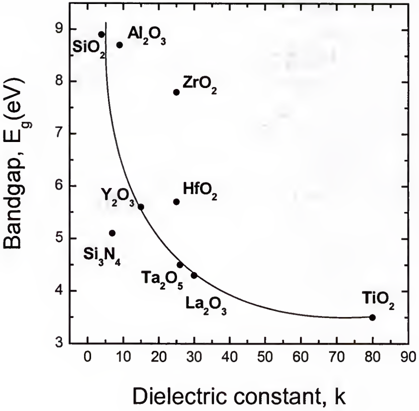


Figure 2-1. High-k gate dielectric candidates

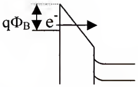
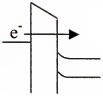
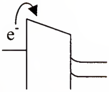
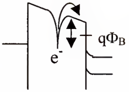
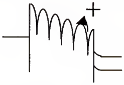
Fowler-Nordheim Tunneling	$J=\frac{A}{4\Phi_B}E_i^2\exp(-\frac{2B\Phi_B^{3/2}}{3E_i})$	
Direct tunneling	$J=\frac{A}{d2}[(\Phi B-\frac{V}{2})\exp(-Bd\sqrt{\Phi B-\frac{V}{2}})$ $-(\Phi B+\frac{V}{2})\exp(-Bd\sqrt{\Phi B+\frac{V}{2}})]$	
Schottky Emission	$J=\alpha T^2\exp(-\frac{\Phi_B-\sqrt{E_i/C}}{\Phi_t})$	
Poole-Frenkel Emission	$J=\alpha E_i\exp(-\frac{\Phi_B-2\sqrt{E_i/C}}{\Phi_t})$	
Ionic Conduction	$J=\alpha\exp(-\frac{\Delta Eae}{kT})$	

Figure 2-2. Typical conduction processes in insulators

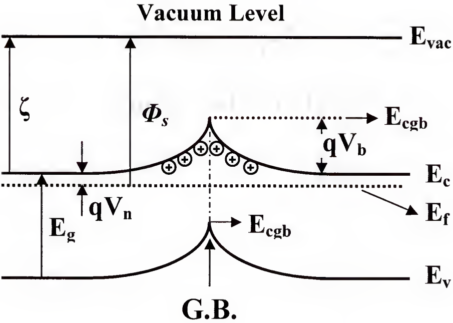


Figure 2-3. Schematic energy band diagram along the n-channel of poly-silicon TFT

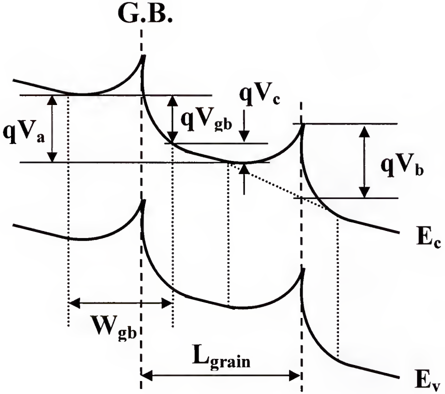


Figure 2-4. Energy band of poly-Si TFT, bias applied, along the channel

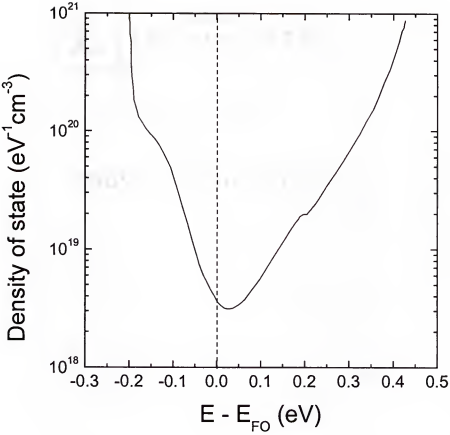


Figure 2-5. Density of states in the forbidden gap for a polysilicon sample

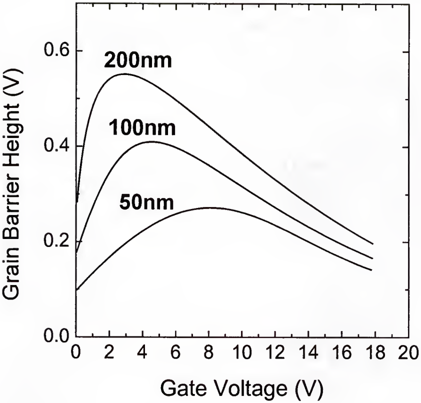


Figure 2-6. The barrier height versus the gate bias for different grain sizes

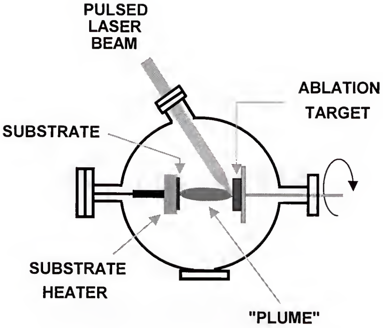


Figure 2-7. Pulsed laser deposition system

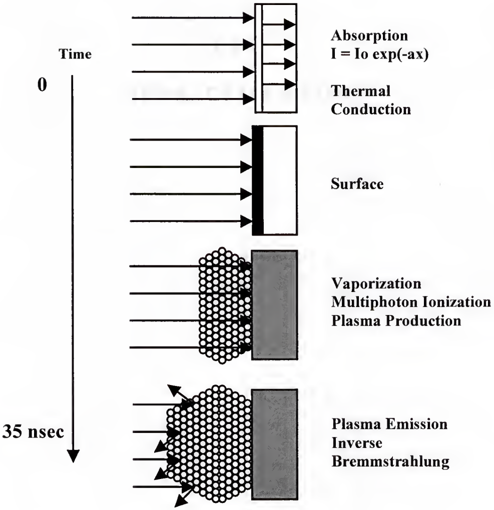


Figure 2-8. Schematic representation of the laser-solid interaction [41]

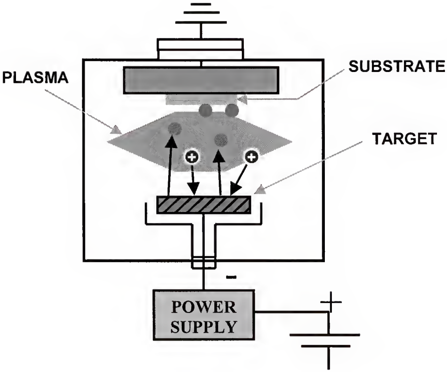


Figure 2-9. Schematic of a dc glow discharge sputtering

CHAPTER 3

EPITAXIAL GROWTH OF CALCIUM HAFNATE THIN FILM ON VARIOUS SUBSTRATES

3.1 Introduction

Since the discovery of high temperature superconductors (HTS) in 1986, significant effort has been directed towards fabricating long, flexible conductors with high critical current densities for a range of applications. A very promising approach for the profitable production of long HTS, $YBa_2Cu_3O_x$ tapes, which are suitable for carrying high currents in magnetic fields is the Rolling Assisted Biaxially Textured Substrates (RABITS^{TM}) method developed at Oak Ridge National Laboratory [42]. A lot of effort has been devoted to construct the structure of HTS using RABITS [43-45]. Unfortunately, direct growth of HTS on substrate is frequently accompanied by chemical reactions or microcrack that degrade the properties of HTS. Therefore, this approach is dependent on the heteroepitaxial growth of oxide buffer layer films between HTS and metal surfaces. Some authors reported about the use of MgO [46,47], YSZ [48,49], $SrTiO_3$ [50,51], sapphire[52,53], Y_2O_3[54], and CeO_2 [55,56]as buffer layers for HTS. CeO_2 has been used to nucleate an epitaxial (001)-oriented oxide layer on a biaxially textured (001) Ni surface. However, the crack between CeO_2 and metal substrate required an additional epitaxial buffer layer on the CeO_2 to achieve crack-free superconducting films [43]. Even if the buffer layer of YSZ on a biaxially textured (001) Ni surface showed no microcracking in the YSZ layer, two in-plane variants of the $YBa_2Cu_3O_7$ film are present.

In order to eliminate one of these in-plane variants, epitaxial capping layer for example, Y_2O_3, and CeO_2 on the YSZ is needed [57].

With replacing the use of a multiplayer buffer architecture that introduce significant complexity to the fabrication process, we used $CaHfO_3$ film on rolling textured Ni and $LaAlO_3$ substrates as buffer layer for HTS.

3.2 Experiments

Pulsed Laser Deposition was used to synthesize $CaHfO_3$ thin films which were grown using an excimer KrF laser with a wavelength of 248 nm. $CaHfO_3$ thin films are grown on Si, Ge, biaxially textured Ni and $LaAlO_3$ substrates.

p-type Si(100) wafers with a resisitivity of 1-10 Ωcm and p-type Ge (100) wafer as the substrates, which were cleaned in a 1:10HF:H_2O solution for 30 s , rinsed in deionized water for 60 s, ultrasonically cleaned with trichloroethylene, acetone, and methanol for 5 min and dried in N_2 to yield a hydrogen-terminated surface respectively. $LaAlO_3$(001) and biaxial textured Ni substrates were cleaned with trichloroethylene, acetone, and methanol for 5 minutes respectively. They were blown dry with nitrogen and mounted on a substrate heater using silver paint. No attempt was made to remove any surface layers prior to loading into the deposition chamber. Upon loading the substrates, the chamber was pumped to a base pressure of $\sim 2\times10^{-6}$ to 5×10^{-6} Torr.

The laser fluence was approximately $\sim 3J/cm^2$ and repetition rate used was 5Hz. Approximately 100nm-thick films were grown at temperatures ranging from 600 to 850 °C at vacuum. Crystal structure was investigated using x-ray diffraction (XRD) with Cu $K\alpha$ radiation (0.15405 nm wavelength).

3.3 Results and Discussion

3.3.1 $CaHfO_3$ on Si

Figure 3-1 (A) shows the XRD patterns of $CaHfO_3$ with 100 nm thickness synthesized at temperatures ranging form 500 to 780°C at vacuum. The patterns show that the crystallized $CaHfO_3$ thin films could not be obtained and still remained as amorphous phase until 780°C.

In order to minimize any native silicon oxide on the substrate surface prior to growth, hydrogen gas was introduced into the chamber. Hydrogen-termination is chemically inactive, especially against oxidation by saturating Si dangling bonds on the surfaces [33]. Herata et al. [34] have used hydrogen-terminated Si (111) as a substrate for heteroepitaxial growth of SrO. Figure 3-1 (B) shows the XRD pattern of $CaHfO_3$ thin film nucleated in ambient of 100mTorr Ar/H_2 and grown at vacuum at the temperature range from 500 to 780°C. As the results, the XRD patterns of $CaHfO_3$ film expected to be nucleated in Ar/H_2 ambient were same to those of film just grown in vacuum and any peak of crystalline could not found.

To improve the crystallinity of the film, more temperature for crystallization was needed up to 850°C and repetition rate was decreased from 5 to 2 Hz. Figure 3-2 shows that the crystallized phases started to appear at the temperature of 800°C and the peak intensity increased when growth temperature was raised. The crystallized phase of $CaHfO_3$ film showing (121) plane appeared at $2\theta=31.8$.

3.3.2 $CaHfO_3$ on Ge

$CaHfO_3$ thin films were grown on Ge substrate at temperatures ranging form 500 to 850°C at vacuum with 100nm-thickness. The XRD patterns of $CaHfO_3$ thin films were exhibited in figure 3-3 (A). The XRD pattern shows that there is no crystallized phase of

$CaHfO_3$ thin films until growth temperature of 700°C. Note that germanium peak and $CaHfO_3$ one have almost same diffraction angle of $2\theta = 31.6$, however, the peak observed at $2\theta = 31.6$ in Figure 3-3 (A) is considered to be related with germanium because it is very difficult to crystallize $CaHfO_3$ thin films at low temperature as seen in the case of using Si substrate. Figure 3-3 (B) shows the XRD patterns of $CaHfO_3$ thin films grown in ambient of 100mTorr Ar/H_2 and grown at vacuum to improve the interface between the germanium substrate and oxide film. However, the quality of the film interface against the substrate is considered to be almost same to that of the film grown at vacuum ambient and we cannot observe the crystallized phase of $CaHfO_3$ film.

Figure 3-4 shows the crystallinity of $CaHfO_3$ thin films grown at the temperatures from 700 to 850°C at vacuum with the repetition rate of 2 Hz which is the value decreased from 5Hz. With increasing the growth temperature, intensity of crystallinity has increased and the peaks of (101) plane and (202) plane have appeared at $2\theta = 22.4$, 45.7 respectively. This XRD patterns exhibit that (101), (202) planes are well developed with increasing the growth temperature at 850°C while these planes were not observed in case of films grown on Si substrates.

3.3.3 $CaHfO_3$ on biaxially textured Ni

An epitaxial oxide thin film serves as an excellent buffer layer for subsequent heteroepitaxy of various functional oxides including high temperature superconductor (HTS). Several factors must be considered in selecting materials for use as buffer layers between substrate and a particular oxide: chemical reactions, interdiffusion, thermal expansion match, crystal structure, and lattice match are some of the most important [35].

In this study, we have grown $CaHfO_3$ thin films on biaxially textured Ni substrate for buffer layer for HTS. Figure 3-5 (A) shows the XRD patterns of $CaHfO_3$ thin films grown at vacuum ambient at the temperature range from 500 to 850°C. the crystallized phases have appeared since we increased the growth temperature from 780°C. With increasing the growth temperature, the peak intensity of (101), (202) planes increased while the peak intensity of (121) plane decreased.

To make hydrogen-terminated surface of Ni substrate, we introduced 100mTorr Ar/H_2 gas into the chamber for easy nucleation. Figure 3-5 (B) shows the crystallinity of the film grown in 100mTorr Ar/H_2 ambient. However, we could not obtained distinct crystallized phases except showing small peak intensity of (121) plane at $2\theta=31.5$.

Figure 3-6 (A) shows the XRD pattern of $CaHfO_3$ thin films grown at the temperatures from 700 to 850°C at vacuum with the repetition rate of 2 Hz. The crystallized phases have appeared at 700°C while on the film grown with the repetition rate of 5 Hz, no crystallized phase has been obtained until 750°C. It could be assumed that the growth of $CaHfO_3$ thin films grown on Ni substrate depends on the repetition rate.

The higher growth temperature, the stronger the peak intensity of (101),(202) planes has been exhibited. Figure 3-6 (B) shows the comparison of peak intensity between (101) and (121) planes with growth temperatures. At high temperature, (101) plane was well developed more than (121) plane.

3.3.4 $CaHfO_3$ on $LaAlO_3$

$CaHfO_3$ thin films have been deposited on lanthanum aluminate $LaAlO_3$ (100) single crystalline substrate. Figure 3-7 shows that the XRD patterns as a function of growth temperatures from 500 to 750°C in the ambient of oxygen partial pressure of 1mTorr. We could obtain the diffraction peaks form the (001), (002) planes of $CaHfO_3$ above 650°C, which indicate the heteroepitaxial growth of $CaHfO_3$ film on $LaAlO_3$ substrate. The observed peaks at 22.27°, 23.47°, 45.41°, 48.05°, 70.57°and 75.15° are identified as CHO(101), LAO(012), CHO(202), LAO(024), CHO(303) and LAO(036) respectively.

Figure 3-8 shows the crystallinity with the ranges of oxygen partial pressure from 10^{-4} to 10^{-1} Torr at the growth temperature of 750°C. A $CaHfO_3$ peaks such as (101), (202), (303) indicating the epitaxial growth is observed in the sample grown at oxygen partial pressure of 10^{-4} Torr and with this condition, no extra XRD peaks from other crystalline orientations of the $CaHfO_3$ film exist in the measured 2 theta range. However, we could observe extra phases like HfO_2 in high oxygen partial pressure. The results indicate that this perovskite oxide heteroeitaxy on $LaAlO_3$ substrate develops with $CaHfO_3(101)$ // $LaAlO_3(100)$.

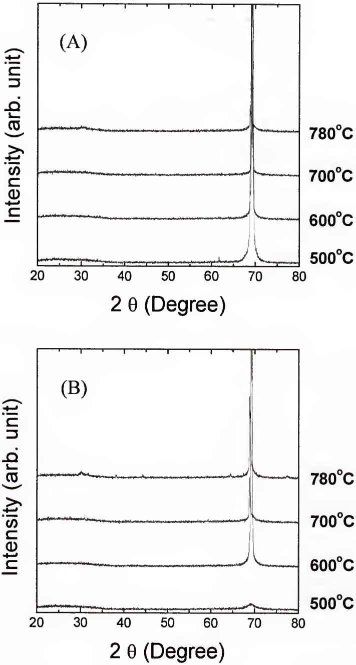


Figure 3-1. XRD pattern of $CaHfO_3$ / Si (A) at temperature ranges from 500 to 780°C at vacuum, (B) nucleated in 100mTorr Ar / H_2 and grown at vacuum with the temperature ranges from 500 to 700°C

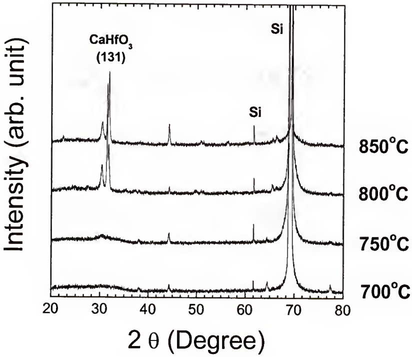
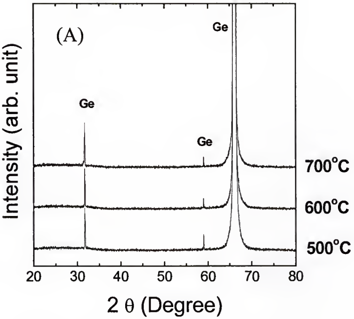


Figure 3-2. XRD pattern of CaHfO$_3$ / Si with the temperature ranges from 700 to 850°C at vacuum with a repetition rate of 2 Hz



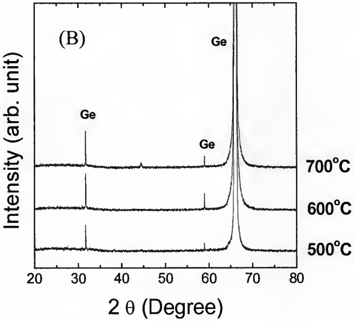


Figure 3-3. XRD pattern of $CaHfO_3$ / Ge grown (A) with the temperature ranges from 500 to 700°C at vacuum, (B) nucleated in 100mTorr Ar/H_2 and grown at vacuum with the temperature ranges from 500 to 700°C

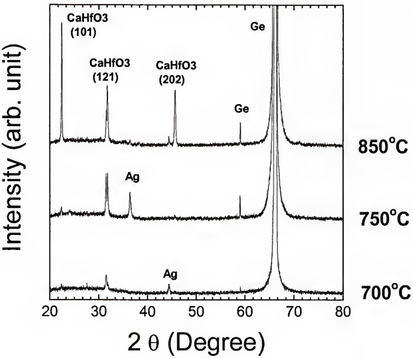


Figure 3-4. XRD pattern of $CaHfO_3$ / Ge at temperature ranges from 700 to 850°C at vacuum with a repetition rate of 2 Hz

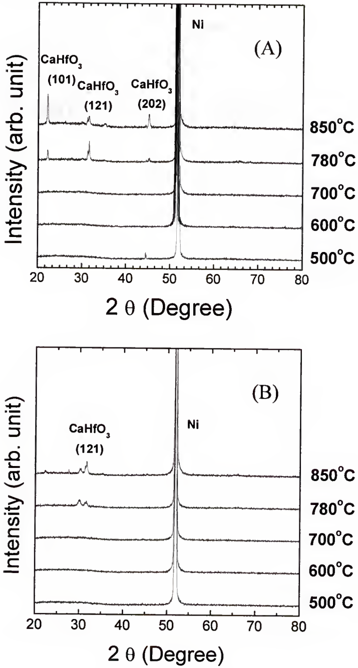


Figure 3-5. XRD pattern of $CaHfO_3$ / Ni (A) with the temperature ranges from 500 to 780°C at vacuum, (B) nucleated in 100mTorr Ar / H_2 and grown at vacuum with the temperature ranges from 500 to 700°C

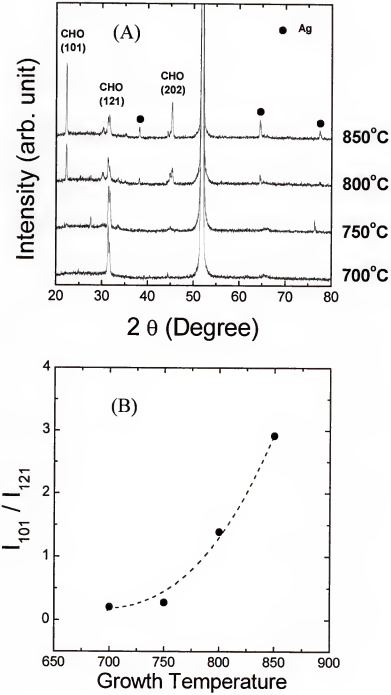


Figure 3-6. XRD pattern of $CaHfO_3$ / Ni with the temperature (A) from 700 to 850°C at vacuum with a repetition rate of 2 Hz, (B) Comparison of peak intensity between (101) and (121) planes

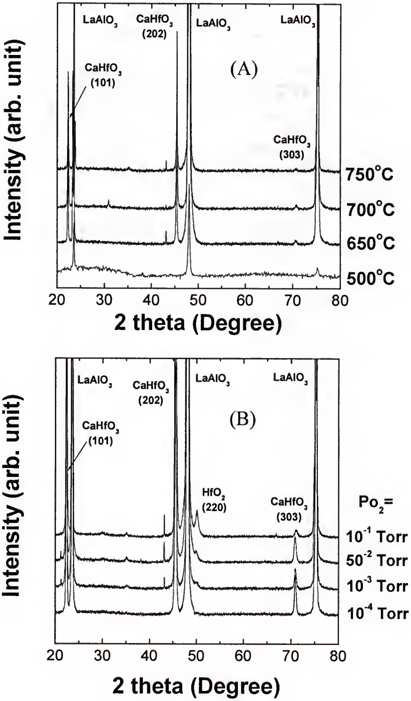


Figure 3-7. XRD pattern of $CaHfO_3/LaAlO_3$ grown at (A) 100mTorr Po_2 as a function of growth temperature from 500 to 750°C, (B) 750°C as a function of oxygen partial pressure from 10^{-4} to 10^{-1} Torr.

CHAPTER 4
RECRYSTALLIZATION AND DIEELECTRIC PROPERTIES OF CALCIUM HAFNATE FILMS ON SILICON

4.1 Introduction

Much of the success of silicon in digital electronic technologies can be directly attributed to the remarkable properties of the Si/SiO_2 interface for metal / insulator / semiconductor (MIS) structures, in which SiO_2 serves as the gate oxide. The structural, electronic, and chemical properties of the SiO_2/Si interface has been extensively investigated for the past quarter century [58]. The performance of silicon-based digital electronics relies on the controlled and understood properties of the SiO_2/Si interface. Yet, the development of future generation high-density, high-speed silicon devices will depend on replacing SiO_2 with an alternative gate insulator that possesses a higher dielectric constant [59]. This is a direct result of the scaling relationships that enable the progressively smaller device structures for higher circuit speeds. Smaller device geometries require higher dopant concentrations in the MOSFET channel region. This, in turn, requires a higher MOSFET gate capacitance/area in order to modulate the channel conductance for switching. The MOSFET gate capacitance can be approximated as a simple parallel-plate capacitor in which the capacitance/area is proportional to the oxide dielectric constant, and inversely proportional to the oxide thickness. Up to the present generation of devices, the required increase in gate capacitance/area has been accomplished by decreasing the thickness of SiO_2. Unfortunately, the gate oxide is rapidly approaching a thickness for which it will no longer function as an effective insulator. Based on the predictions of Moore's law, the current 0.18 μm minimum line width integrated microelectronic technology will progress to less than 0.10 μm within the next 6–8 years. For 0.1 μm line width technology, the required capacitance/area for the MOSFET gate dielectric will approach 35 fF/μm^2. For SiO_2, this translates into a dielectric thickness of approximately 1.0 nm. At this thickness, quantum-mechanical tunneling currents through the oxide will yield a gate leakage current in excess of 1 A/cm^2, which is unsuitable for MOSFET circuit operation. This anticipated failure of SiO_2 will require the development of an alternative gate dielectric material that satisfies the challenging metrics for device performance.

The alternative gate dielectric structure must be compatible with subsequent device processing while demonstrating high capacitance/area, low interface trap density and low leakage current [60-62]. Capacitance is limited more by interfacial reactions between the dielectric and silicon than by the dielectric constant of the deposited oxide, since a SiO_2 interface layer of only 1 nm imposes an upper limit of ~35 fF/cm^2 for the gate capacitance. Leakage current is determined by the insulator bandgap, resistivity of the insulator, dielectric breakdown, and the bandgap offset relative to the semiconductor. It is also dependent on dielectric microstructure, with grain boundaries providing regions of locally high fields and/or high conductance. Interface trap states are generally associated with dangling bonds at the oxide/semiconductor interface. These requirements have proven difficult to satisfy for deposited gate dielectrics. High permittivity generally correlates with small bandgaps, yielding higher leakage currents. Thermal processing of device structures typically leads to polycrystalline grain growth. Controlling interface states for deposited dielectrics is poorly understood. In terms of interface stability, the most insightful contribution is that from Schlom et al. who examined the thermodynamic stability of binary oxides on silicon in an effort to theoretically predict which oxides are less susceptible to interfacial reactions [63]. This approach provides a reasonable framework for considering binary oxide deposition on semiconductors, and lends some guidance in addressing the utility of ternary and quaternary oxide compounds.

In recent years, significant activity has been directed at the synthesis and properties of various oxides on Si. Oxide thin films investigated as potential gate dielectrics include a number of binary and ternary systems, including HfO_2 [64,65] yttria stabilized zirconia [66], Y_2O_3 [67], MgO [68], CeO_2 [69], and $(Sr,Ba)TiO_3$ [70,71]. At present, one of the most promising gate dielectric materials is HfO_2. Hafnium oxide exhibits a dielectric constant of ~30 and a band gap 5.6 eV. Both experimental and theoretical evidence suggest that the HfO_2/Si interface is thermodynamically stable against the formation of silicides. HfO_2-based MOS capacitors have been fabricated with a HfO_2 layer thickness of 4.5 nm, yielding an capacitance/area approaching 35 fF/μm^2 and a leakage current of only 3×10^{-2} A/cm^2 at a gate voltage of −1.5 V [72]. A potential limitation to using HfO_2 as the gate oxide in functional devices is the relatively low recrystallization temperature (~650 °C) for an amorphous to polycrystalline transformation [73]. We have investigated the properties of amorphous $CaHfO_x$ films as they pertain to their use as gate dielectrics. $CaHfO_3$ is a pseudo-cubic perovskite possessing an orthorhombic crystal structure, with lattice parameters a=5.568 Å, b=5.732 Å, and c=7.984 Å. The refractive index of $CaHfO_3$ was measured to be $<n>$=2.00 at a wavelength of 500 nm. $CaHfO_x$ is an interesting gate dielectric candidate material on Si as both the A- and B-site cation sub-oxides are thermodynamically stable in contact with Si. Arguments based on the change in the

Gibbs free energy suggest that both CaO and HfO_2 in contact with Si are likely stable against silicide formation up to 1000 °C. The focus of this study was to investigate the thermal stability of the amorphous $CaHfO_x$ structure relative to HfO_2, determine the dielectric properties of $CaHfO_x$ amorphous thin films, and explore the formation and properties of $CaHfO_x$-based metal–insulator–semiconductor (MIS) structures.

4.2 Experiments

$CaHfO_x$ thin films were synthesized on Si (0 0 1) by pulsed laser deposition using an KrF excimer laser with a wavelength of 248 nm. P-type Si (1 0 0) with a resisitivity of 1–10 Ω cm were ultrasonically cleaned with trichloroethylene, acetone, and methanol for 5 min and cleaned in a 1:10HF:H_2O solution for 30 s, rinsed in deionized water for 60 s, and dried in N_2 to yield a hydrogen-terminated surface. Substrates were mounted on a substrate heater using silver paint. Upon loading the substrates, the chamber was pumped to a base pressure of ~2–5 × 10^{-6} Torr. A laser with an energy density of ~3 J/cm^2 was focused on a stoichiometric $CaHfO_3$ ceramic target with pulse frequency of 5 Hz. The distance between the target and the substrates was fixed at 6 cm. $CaHfO_x$ thin films were deposited at various oxygen partial pressure and substrate temperatures. The majority of the results reported in this paper are for an oxygen partial pressure of 10^{-1} Torr and substrate temperature of 100 °C. The thickness of oxide films was varied from ~20 to 200 nm. Recrystallization behavior was investigated using 200 nm films annealed in air. Film crystallinity was determined using X-ray diffraction. Capacitors with a MIS structure were fabricated using as-deposited $CaHfO_x$ films and 200 nm diameter Pt gate electrodes deposited using DC magnetron sputtering. Ag was used as the backside metal electrode. Capacitance–voltage (*C–V*) characteristics were measured at frequencies of 100 kHz and 1 MHz. Current–voltage (*I–V*) characteristics were measured as well.

4.3 Results and Discussion

Initial activities focused on the relative stability of amorphous $CaHfO_x$ when annealed in air. Previous work investigating rapid thermal annealing of HfO_2 indicated an onset of recrystallization behavior at approximately 650 °C. In contrast, polycrystalline grain formation did not become apparent in $CaHfO_x$ films annealed in air for 60 min. until an annealing temperature of ~800 °C was employed. Figure 4-1 shows the X-ray diffraction patterns for $CaHfO_x$ annealied at various temperatures. Polycrystalline peaks are not evident until an annealing temperature of 850 °C is reached. It is well known from the behavior of glasses that additional cations can frustrate the long-range ordering needed for crystallization to proceed [74]. For $CaHfO_x$, grain growth depends on the long-range ordering of Ca and Hf cations. This requires more diffusion than the simple formation of HfO_2 in the fluorite structure. In order to further delineate the crystallization behavior of $CaHfO_x$, films were also deposited at elevated substrate temperatures. This sets an lower limit to the onset of recrystallization as in situ deposition on a heated substrate minimizes solid-state diffusion processes needed for grain growth. X-ray diffraction results for $CaHfO_x$ films deposited at various temperatures are shown in figure 3-2. In this case, polycrystalline peaks first appear for a deposition temperature of 800 °C. It is most probable that much higher temperatures would be needed to observe recrystallization in $CaHfO_x$ when rapid thermal annealing is employed.

The stability of amorphous calcium hafnate thin films was also compared with related zirconate and cerate compounds. Zirconates and cerates have similar chemistry as that of the hafnate compounds. In particular, $BaZrO_x$ and $CaCeO_x$ thin films were deposited at room temperature and annealed in air for 60 min at annealing temperatures of 500–1000 °C. The X-ray diffraction results for $BaZrO_x$ are shown in figure 4-2. In the case of $BaZrO_x$ thin films, evidence for polycrystalline grain formation emerges at 700 °C, indicating that the amorphous phase of calcium hafnate is more stable than that of barium zirconates at high temperature process. Similar results were observed for $CaCeO_x$.

In order to determine the dielectric constant for $CaHfO_x$, the capacitance–voltage (C–V) characteristics for MIS structures possessing various film thicknesses were measured from accumulation to depletion. Figure 4-3 shows a plot of $1/C$ values extracted from the accumulation region as a function of film thickness. This allows one to delineate the dielectric properties of the deposited film from any interfacial layer. Assuming that the effective capacitance is due to the $CaHfO_x$ thin film in series with an interfacial layer (presumably SiO_2), the total capacitance is given by

$$\frac{1}{C_{tot}} = \frac{d}{\varepsilon_o \varepsilon_r A} + \frac{d'}{\varepsilon_o \varepsilon' A}$$

In this expression, d and d' are the thicknesses of $CaHfO_x$ film and SiO_2, respectively, A is the electrode area, ε_0 is the permittivity of vacuum, ε' is the relative permittivity of SiO_2, and ε_r is the relative permittivity of $CaHfO_x$. Since the films are deposited at low temperature, we assume that the interfacial layer thickness is independent of $CaHfO_x$ layer thickness. This assumption is confirmed by the linear relationship between $CaHfO_x$ thickness and $1/C_{tot}$. Based on the slope of $1/C_{tot}$ plotted as a function of deposited film thickness, the dielectric constant of the $CaHfO_x$ thin film is determined to be 13. This value is somewhat lower than that of other candidate gate dielectric materials, although its utility will depend on the interfacial layer. From the extrapolated intercept of $1/C_{tot}$ for a $CaHfO_x$ thickness of zero, the interfacial capacitance is 40 $fF/\mu m^2$, assuming no quantum-mechanical corrections. Assuming that the interfacial layer is SiO_2, the interfacial layer thickness between $CaHfO_x$ film and Si substrate is 8.6

Å. No attempt has been made to optimize processing conditions as to minimize interfacial capacitance.

The C-V measurements also provide the flatband information of the MOS device. To measure the flatband voltage, it is necessary to determine the flatband capacitance. With the structure of dielectric stack including a SiO_2 bottom layer and a high-k alternative gate dielectric top layer, the flatband capacitance, C_{FB}, normalized by C_{ox} is given as [75]

$$\frac{C_{FB}}{C_{ox}} = \frac{1}{1+\frac{C'}{C_s}} = \frac{1}{1+\frac{3.57\times10^{-5}}{(1.12\times10^{-6})+(3.9\times d)}}$$

where $1/C' = 1/C_{ox} + 1/C_{SiO2}$, and d is the thickness of $CaHfO_3$. From the equation, the flatband voltage is calculated with an each thickness of $CaHfO_3$, and expressed as a function of $CaHfO_3$ thickness shown in figure 4-4. If the interface traps play a negligible role in fixed charge density measurements, the flatband voltage can be given by

$$V_{FB} = \phi_{MS} - \frac{Q_f}{C_{ox}} = \phi_{MS} - \frac{Q_f}{K_{ox}\varepsilon_0} d$$

where Q_f is the fixed charge in Si, K_{ox} is the dielectric constant of oxide, and ϕ_{MS} is the metal / semiconductor work function difference. The fixed charge density is determined to be 7.49 x $10^{11}/cm^2$ from the slope in figure 4.4. From the extrapolated intercept of flatband voltage for a $CaHfO_x$ thickness of zero, the metal / semiconductor work function difference is 0.104 V.

As seen with other deposited oxide dielectrics [76,77], there can be significant hysteresis in the capacitance measurement for as-deposited $CaHfO_x$ films as the gate voltage is cycled through positive to negative values. Figure 4-5 shows *C–V* measurements, cycled through accumulation to depletion, taken at different sweep rates at a measurement frequency of 1 MHz. The degree of hysteresis in the *C–V* curves depends on the sweep rates used for the measurements. Similar results have been observed in other dielectrics and attributed to the presence of mobile ions in the $CaHfO_x$ films. With increasing sweep rates, the hysteresis in capacitance increased, which is consistent with an ion relaxation time constant that is large as compared to the sweep rates. The hysteretic behavior observed in the measurements is consistent with the presence of mobile ions in the $CaHfO_x$ dielctric film. Future work will focus on understanding the origin of the mobile charge density in the $CaHfO_x$ film.

In addition to *C–V*, we also investigated the leakage current behavior of as-deposited films as seen in figure 4-6. A relatively high leakage current ($\sim10^{-3}$ A/cm^2 at 1 V bias for a 20 nm $CaHfO_x$ film) was observed. The leakage current may reflect non-stoichiometric films ($x<3.0$), or may be the result of inherent particulates from the PLD process leading to pinholes, as no effort was made to reduce or eliminate particulate density.

4.4 Conclusions

The recrystallization and dielectric behavior for amorphous $CaHfO_x$ films on Si substrate has been investigated. Upon conventional annealing in air, the $CaHfO_x$ films remain amorphous up to an annealing temperature of 800 °C for annealing times of 1 h. This recrystallization temperature is significantly higher than that reported for HfO_2 subjected to rapid thermal annealing. Metal–insulator–semiconductor structures with Pt gate electrodes were fabricated with various $CaHfO_x$ film thickness for capacitance–voltage (C-V) and leakage current (I-V) measurements. From this, the permittivity of $CaHfO_x$ was determined, along with interface layer capacitance for films on Si. The enhanced stability against polycrystalline grain growth, along with the thermodynamic stability of both CaO and HfO_2 in contact with Si, suggests that $CaHfO_x$ may be an attractive gate dielectric for future generation metal–oxide–semiconductor field-effect transistor applications.

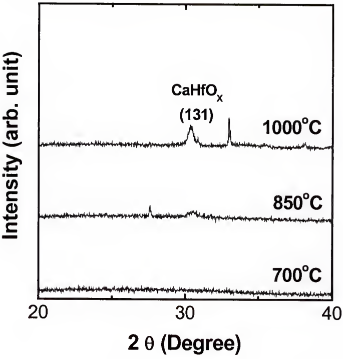


Figure 4-1. X-ray diffraction data for CaHfO$_x$ films deposited at low temperature and annealed at high temperature in air. Annealing time was 1 h.

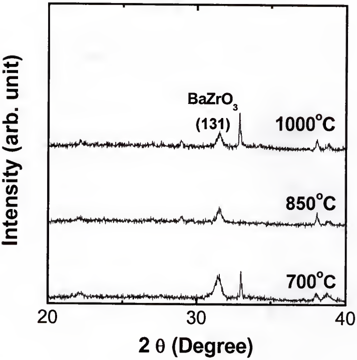


Figure 4-2. X-ray diffraction data for $BaZrO_x$ films deposited at low temperature and annealed at high temperature in air. Annealing time was 1 h

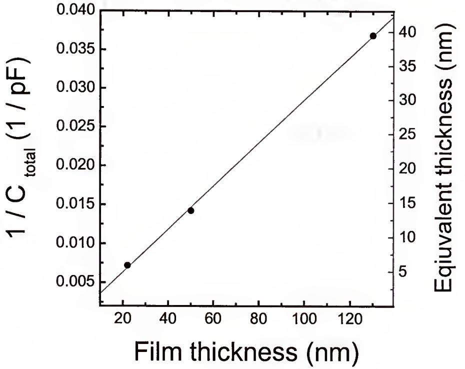


Figure 4-3. Plot of the inverse total capacitance as a function of $CaHfO_x$ film thickness for as-deposited films

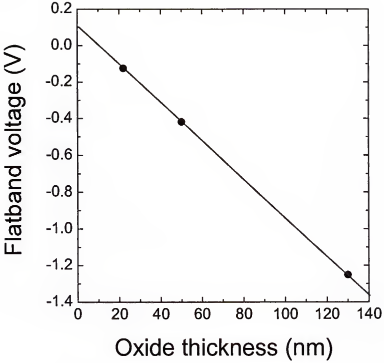


Figure 4-4. Flatband voltage of Al/$CaHfO_3$/Si MOS device as a function of $CaHfO_3$ thickness

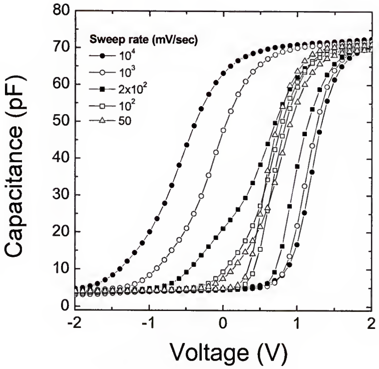


Figure 4-5. *C–V* measurement for CaHfO$_x$-based MIS capacitors taken with different sweep rates

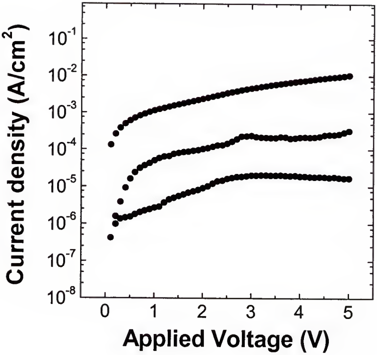


Figure 4-6. Leakage current measurements for CaHfO$_x$ MIS capacitors with different gate oxide thicknesses

CHAPTER 5
DIELECTRIC PROPERTIES OF AMORPHOUS WIDE BANDGAP ALUMINATE FOR GATE OXIDE

5.1 Introduction

In recent years, pulsed laser deposition has emerged as an enabling technique in oxide thin-film research. It has been implemented in materials and device research involving a number of different oxide material classes, including the deposition of oxides as gate dielectric in field-effect device structures [78-82]. However, one area where pulsed laser deposition has limitations is in the formation of ultra-high band gap insulators, particularly as these relate to the formation of electric field-gated device structures.

There has developed significant interest in the formation of electric field-gate structures of various field-effect channel materials. For the electric field gating of wide bandgap semiconductors, the band gap of the gate oxide material must be necessarily large to as to prevent the injection of charge into the channel through the gate oxide valence or conduction band. As such, gate dielectrics must have very large band gaps. In addition, the gate oxide must be pinhole free and preferably amorphous so as to prevent leakage through grain boundaries. For the deposition of gate dielectrics using pulsed laser deposition, these ultra-wide band gap dielectrics present a significant challenge. Pulsed laser deposition is dependent on an optical absorption process that yields ablation of the target. For ultra-wide gap materials, ablation is dependent on absorption via crystalline defects in the ablation target. Unfortunately, this is quite inefficient and yields significant particulate densities that are detrimental to the performance of a gate dielectric. In addition, the energetics of the pulsed laser deposition process promotes crystallization of the deposition film which is often not desirable.

In the paper, we describe an approach that circumvents this limitation. In particular, the deposition of a multi-cation $Ce_{0.33}Tb_{0.67}MgAl_{11}O_x$ amorphous films utilizing pulsed laser ablation of luminescent $Ce_{0.33}Tb_{0.67}MgAl_{11}O_{19}$ sintered targets are described. The dielectric properties of the $Ce_{0.33}Tb_{0.67}MgAl_{11}O_x$ amorphous films are discussed within the context of their use as a gate dielectric.

5.2 Experiments

The ablation targets were fabricated from commercial $Ce_{0.33}Tb_{0.67}MgAl_{11}O_{19}$ phosphor powders (Stanford Materials). Crystalline $Ce_{0.33}Tb_{0.67}MgAl_{11}O_{19}$ is an efficient green phosphor with a strong absorption at ~253.7 nm [83-87]. The powders were pressed into 1 inch targets and annealed in air at 1200°C for 14 hours, 1400°C for 14 hours, and at 1500°C for 24 hours. The targets displayed bright green luminescence when exposed to 254 nm ultraviolet light. The $Ce_{0.33}Tb_{0.67}MgAl_{11}O_x$ amorphous films were deposited in a conventional pulsed laser deposition system (base pressure 10^{-6} Torr) using a KrF 254 nm excimer laser as the ablation source. The strong absorption at 254nm yields an efficient laser ablation process with virtually no particulate ejection from the target. The films for gate dielectric measurements were deposited at 100°C in 1mTorr. X-ray diffraction of the films showed no evidence of crystallinity. Figure 5-1 shows a field-emission scanning electron microscopy (SEM) image of a $Ce_{0.33}Tb_{0.67}MgAl_{11}O_x$ amorphous film deposited on ITO-coated glass. Note that there is no evidence for particulates on the surface. The lateral structure seen in the image is the grain structure of the ITO polycrystalline film. Several multiplayer structures have been realized. Figure 5-2 shows a cross-section scanning electron microscope image of a Si/SiO$_2$/Ti/Pt/ZnO/ Ce$_{0.33}$Tb$_{0.67}$MgAl$_{11}$O$_x$ multilayer stack. The grain structure is clearly evident in the (Zn,Mg)O and Pt layers, but no grain structure is seen in the Ce$_{0.33}$Tb$_{0.67}$MgAl$_{11}$O$_x$ layer.

For the gate dielectric measurements, metal-insulator-metal (MIM) diodes were fabricated using Al for the top electrode and indium tin oxide (ITO) coated on glass for the bottom electrodes. The thickness of ITO on the glass was 100 nm. The CTMA films grown on the ITO coated glass by pulsed laser deposition had a thickness of 100 nm. In addition to MIM diode, metal-insulator-semiconductor (MOS) diodes were fabricated using p-type Si. The growth conditions were same to the cases of MIM fabrication. Aluminum was deposited by magnetron sputtering at room temperature for the top electrode. The diameter of the diodes was 200 μm using metal shadow masks. Current-voltage (I-V) characteristics were performed at temperatures up to 573 K in air. The capacitance and conductance of the diodes was measured with the frequency sweep from 100Hz ~ 1MHz.

5.3 Results and Discussion

Figure 5-3 shows the I-V characteristics of the MIM diode measured at 25°C. The leakage current density for CTMA films was very low, measured at room temperature to be ~10^{-6}A/cm^2 at an applied field of 5MV/cm. From the capacitance measurements, the dielectric constant for the amorphous CTMA was determined to be ~ 10, which is similar to that of Al$_2$O$_3$. In order to explore the mechanism of leakage current in the CTMA films, temperature-dependent I-V measurements were performed. The I-V characteristics on MIM diodes were measured from 298K to 573K are shown in figure 5-4. Note that log of the leakage current density is linear with respect to the square root of the applied electric field. This holds true for all temperatures, indicating that the leakage current behavior is consistent with the Schottky emission model [88,89]. The Schottky equation can be written as

$$J = A^* T^2 \exp(-\frac{\Phi_B}{kT}) \exp(\beta \sqrt{E_o})$$

$A^* = (4\pi e m^* k^2/h^3)$

In this equation, J is the current density, $\beta = (e/kT)(e/4\pi\varepsilon_0\varepsilon)^{1/2}$,ε_0 is the permittivity of free space, ε is the optical dielectric constant, E_0 is the electric field at the metal/insulator interface, e is the electronic charge, k is the Boltzmann constant, h is the Planck constant, ϕ_b is the barrier height at the cathode, $A^*$is the Richardson constant, and m* is the effective electron mass.

Figure 5-5 shows a plot of $\ln(J/T^2)$ as a function of 1/T. The Schottky emission mechanism should be most dominant at high temperature and low electric field in order to prevent image field that lowers the potential barrier. Therefore, the Schottky barrier was calculated from data taken in the temperature range 200 to 300°C for the applied voltages between 0.4 and 3V. From this, the Schottky barrier was estimated to be 0.52 eV. However, mean free path of the charge is equal to or less than the thickness of insulator. Note that the thickness of CTMA 100 nm is likely greater than the mean free path of the charge. To extract a more exact barrier height, the modified Schottky equation suggested by Simmons [90] should be used.

$$J = \alpha\ T^{3/2} E_0\ \mu (m^* / m_0)^{3/2} \exp(-\frac{\Phi_B}{kT}) \exp(\beta \sqrt{E_o})$$

In addition to measurements of single CTMA layers, the dielectric properties of multi-layered CTMA/$SrTiO_3$ (STO) were also investigated. $SrTiO_3$ has a much higher dielectric constant than CTMA, but suffers from high leakage current when deposited at low temperature using pulsed laser deposition. Figure 5-6 shows the schematic cross-sectional view of the MIM structure. The CTMA deposited on ITO creates a leakage current barrier to the electrode and STO deposited on CTMA increases the dielectric constant of multi-layered insulator relative to a comparable thickness of CTMA. The thickness of CTMA and STO is designated T_1 and T_2, respectively. The total dielectric constant of the multi-layered stack can then be written as,

$$\varepsilon_{tot} = \frac{\varepsilon_{r2}}{1 + (1 - \frac{T_2}{T_1})(\frac{\varepsilon_{r2}}{\varepsilon_{r1}} - 1)}$$

where ε_1 and ε_2 is the dielectric constant of CTMA and STO, respectively. Figure 5-7 shows the modulation of dielectric constant as a function of thickness of STO. The dielectric constants of multi-layered insulators were calculated, indicating that dielectric constants depend on the thickness of insulator with high dielectric constant. Multi-layered insulators were synthesized with different ratios of STO and CTMA thickness. Total thickness of multi-layered insulator was fixed at 150nm. The dielectric constant of insulator increased with the ratio of thickness of STO. The measured values are very close the calculated values. Figure 5-8 shows the leakage current density of insulator, measured at room temperature. Future experiments will address CTMA/STO laminates in which the CTMA layer is used for leakage current and the STO is used for high dielectric constant.

In order to investigate dielectric properties of $Ce_{0.33}Tb_{0.67}MgAl_{11}O_x$ amorphous film on semiconducting layer, the metal/insulator/semiconductor multilayer stack was fabricated using p-type silicon. Figure 5-9 showed the cross-sectional SEM image of MOS structure. The thickness of $Ce_{0.33}Tb_{0.67}MgAl_{11}O_x$ amorphous film was 100nm. There is no inherent particulate from the PLD process leading to pinholes and no grain structure is seen in the $Ce_{0.33}Tb_{0.67}MgAl_{11}O_x$ layer.

Figure 5-10 shows the I-V characteristics at room temperature from Al/dielectric/Si diode with electrode area of 3.14×10^{-4} cm^2. The leakage current densities were on the order of 10^{-7} A/cm^2 with the reverse and forward biases of ±5MV/cm. Capacitance-voltage characteristics were measured at 1MHz shown in figure 5-11. The dielectric constant with 100nm was determined to be 10 from the accumulation region which is in agreement with the value of Al_2O_3. Because the high frequency capacitance is related to oxide capacitance and semiconductor capacitance, the flatband voltage was estimated to be –0.54V. The interface trap density was obtained using Terman method [91]. Due to the stability of native oxide on the surface of Si, SiO_2 exists between Si and $Ce_{0.33}Tb_{0.67}MgAl_{11}O_x$ layer. The interface trap density on the surface of Si can be extracted from the facts that interface traps do not respond to the ac voltage in high frequency C-V measurements while they follow changes in applied bias. Therefore high frequency capacitance can be expressed as $C_{HF} = (C_{ox}C_s)/(C_{ox}+C_s)$. The comparison between theoretical plot of C_{HF} and measured plot of C_{HF} generates the relationship between band bending, Ψ_s, and applied voltage, V. The interface capacitance, $C_{it}(\Psi_s)$, can be determined from the derivative $d\Psi_s/dV$ given by

$$C_{it}(\Psi_s) = \left[\left(\frac{d\Psi_s}{dV} \right)^{-1} - 1 \right] - C_s(\Psi_s)$$

The interface trap density of MIS diode was determined to be ~1×10^{12} eV^{-1} cm^{-2} from the equation of $C_{it}(\Psi_s) = qD_{it}$. This Terman method is generally considered to be useful for underestimating interface trap density due to its limitation of insufficient high frequencies.

The interface trap density can also determined from conductance method [92,93] using the process, that is, the capture and emission of carriers by interface states in the silicon space-charge region. This capture and emission of majority carriers causes an energy loss observed at all frequencies. The energy loss is related with the conductance. The conductance and capacitance of MIS diode using Si substrate was obtained with the frequency sweep from 100Hz~1MHz. Figure 5-12 shows the conductance versus frequency curves for four different bias voltages at room temperature. The interface trap density was determined to be ~3×10^{12} eV^{-1} cm^{-2} with the equation given by

$$\frac{<G_p>}{\omega} = \frac{\omega C_{ox}{}^2 G_m}{G_m{}^2 + \omega^2 (C_{ox} - C_m)^2}$$

where G_m and C_m represent the measured conductance and capacitance of the MIS device, respectively, C_{ox} is the oxide capacitance in the accumulation, and ω is the angular frequency. Interface trap densities from conductance method were obtained at $E-E_v= 0.6$ eV, and was compared with those from Terman method shown in figure 5-13. Interface trap densities using conductance method have higher value than those with Terman method.

5.4 Conclusions

The dielectric properties of $(Ce,Tb)MgAl_{11}O_x$ films deposited by pulsed-laser deposition are reported. Films deposited at room temperature are amorphous. MIS and MOS device structures are fabricated for dielectric and leakage current measurements. The relative dielectric constant of this aluminate is on the order of 10. Leakage current density was as low as 6×10^{-8} A/cm^2 at the applied voltage of 5V and the conduction mechanism was determined to be Schottky emission model on ITO substrate. The interface trap densities between insulator and Si were $\sim1\times10^{12}$ eV^{-1} cm^{-2} and $\sim3\times10^{12}$ eV^{-1} cm^{-2} using Terman method and conductance method, respectively. The UV optical absorption for this material makes its efficient for pulse-laser deposition employing a UV laser source.

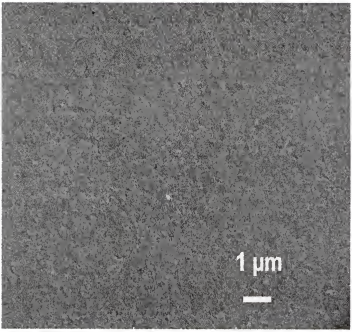


Figure 5-1. SEM image of a $Ce_{0.33}Tb_{0.67}MgAl_{11}O_x$ film on ITO-coated glass

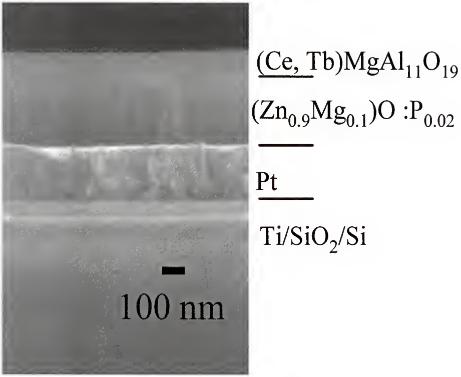


Figure 5-2. Cross-section SEM image of a Si/SiO_2/Ti/Pt/ZnO/ $Ce_{0.33}Tb_{0.67}MgAl_{11}O_x$ multilayer stack

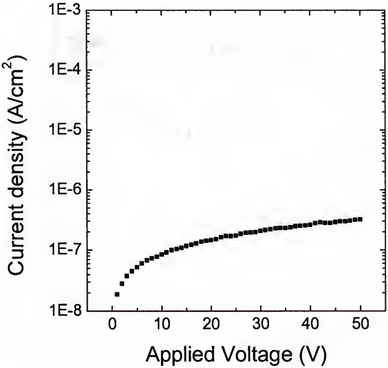


Figure 5-3. I-V characteristics of Al / CTMA / ITO structure with electrode area of 3.14×10^{-4} cm^2

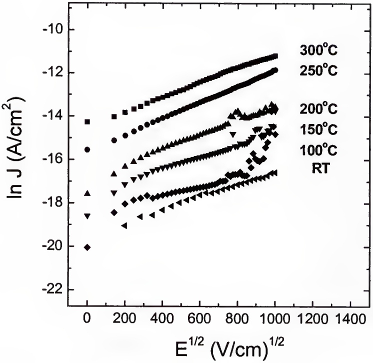


Figure 5-4. Voltage dependence of the steady-state current density from 298 to 573K

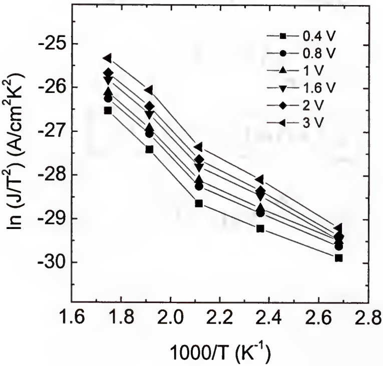


Figure 5-5. $\ln(J/T^2)$ vs $1/T$ as a function of applied voltages from 0.4 to 3V

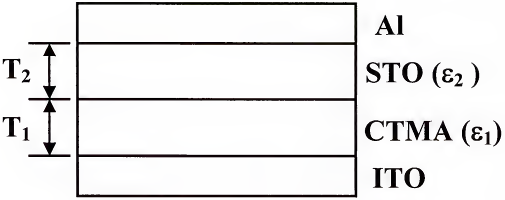


Figure 5-6. Schematic cross-sectional view of multi-layered insulator with metal/insulator/metal structure

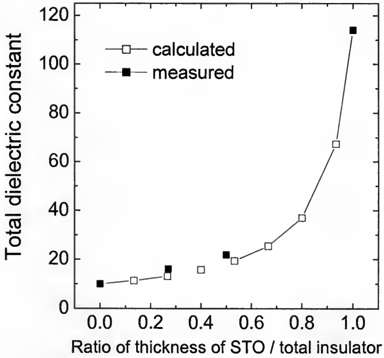


Figure 5-7. Dielectric constant of multi-layered insulator with the ratio of thickness of STO to total insulator

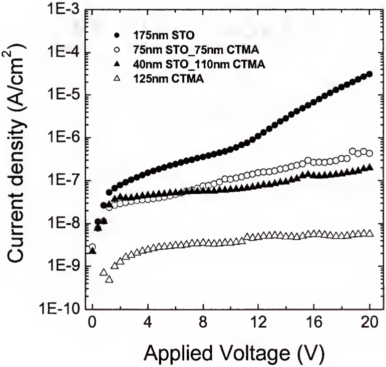


Figure 5-8. I-V characteristics of multi-layered insulator measured at room temperature

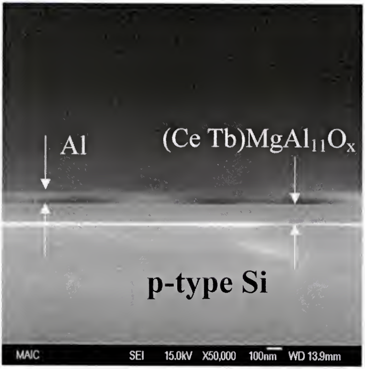


Figure 5-9. Cross-sectional SEM image of Al / $Ce_{0.33}Tb_{0.67}MgAl_{11}O_x$ / Si structure

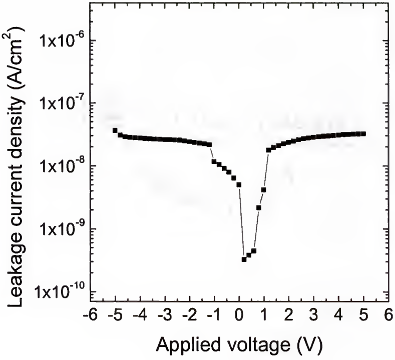


Figure 5-10. I-V characteristics at room temperature from Al/dielectric/Si diode with electrode area of 3.14×10^{-4} cm^2

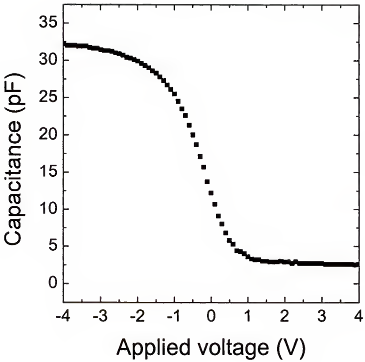


Figure 5-11. Capacitance-voltage characteristics measured at 1MHz with electrode area of 3.14×10^{-4} cm^2

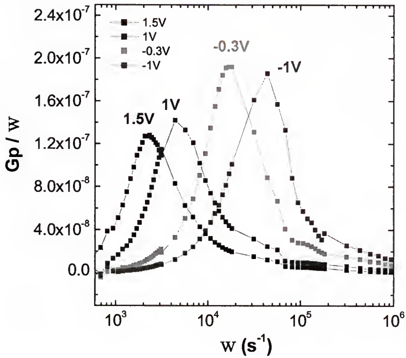


Figure 5-12. Conductance versus frequency curves for four different bias voltages at room temperature

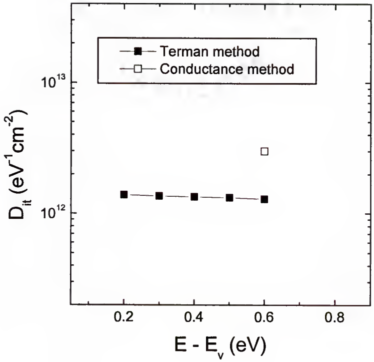


Figure 5-13. Comparison of interface trap density from the conductance method and Terman method

CHAPTER 6

DEPLETION MODE THIN-FILM FIELD-EFFECT TRANSISTORS USING UNDOPED AND PHOSPHOROUS-DOPED ZNO CHANNEL

6.1 Introduction

ZnO is a transparent conducting oxide with wide optical band gap, high electrical conductivity and optical transmittance in the visible region. Undoped ZnO is an n-type and II-VI compound semiconductor with a direct band gap of 3.35 eV. N-type behavior is caused by oxygen vacancies or excessive Zn resulting in the intrinsic defect levels below the conduction band. The Hall mobility of ZnO single crystals at room temperature is on the order of 200 $cm^2V^{-1}s^{-1}$ [94]. Recently, n-type ZnO thin film was achieved by molecular beam epitaxy [95], radio-frequency (rf) sputtering [96], and hybrid beam deposition [97].

With transparent semiconducting properties of ZnO, transparent field-effect transistors (TFETs) based on ZnO as an active channel layer was realized [37-39]. Hoffman *et al* reported that bottom-gate-type thin film transistor was fabricated using undoped ZnO as an active channel deposited via ion beam sputtering. Their device operated as an n-channel enhancement-mode TFT and its effective channel mobility and threshold voltages were found to be 0.35-0.45 cm^2/V s and 10-15 V, respectively. Another enhancement-mode TFT using undoped ZnO for the active channel was reported by Carcia *et al.* The bottom-gate ZnO-TFT with channel length of 20μm was fabricated using rf sputtering. Masuda *et al* fabricated an n-channel depletion-mode TFT with undoped ZnO for the channel. ITO served as the source, drain, and gate and, SiN_x acted as the gate insulator.

One of the major challenges in ZnO-based FET development is to control the carrier density in the active channel. As-deposited ZnO films tend to display a high carrier density, even for materials that are nominally undoped. In order to enhance the electrical performance in the FET, the channel with low carrier concentration is desirable for the operation of device. For the polycrystalline ZnO-based TFT with nano-scaled grains, the enhancement mode TFT is realized with not only low carrier density of the channel but also double Schottky barrier formed near grain boundaries. With high carrier concentration of channel, the depletion mode TFT is achieved because a high carrier density yields a channel that will be conducting in the absence of applied gate voltage. To widely deplete the carriers in the channel with the applied gate voltage, small carrier density is desired for the performance of depletion-mode TFT.

In this article, we report the fabrication and electrical characteristics of n-type depletion-mode TFTs with top gate structure. Undoped and phosphorous-doped ZnO were used for active channel layer. Recently, it has been shown that phosphorus substitution introduces an acceptor level that reduces the electron density or, in some case, yields *p*-type behavior. Amorphous $(Ce,Tb)MgAl_{11}O_x$(CTMA) and HfO_2 served as the gate oxide for TFT using undoped ZnO and phosphorous doped ZnO, respectively.

6.2 Experiments

Metal-oxide-semiconductor (MOS) diodes were synthesized using undoped ZnO thin films as the semiconducting oxide. ZnO was deposited on the substrates of ITO coated glass by Pulsed Laser Deposition (PLD). The growth temperature was 400°C and the oxygen partial pressure was 20 mTorr. In order to characterize the electrical properties of MOS diode, CTMA and Al were served as a gate oxide and a top electrode, respectively.

For the fabrication of transistors, the substrates used for these devices were indium-tin-oxide (ITO)-coated glass. Prepatterned ITO pads serve as the source and drain regions. Undoped and 2 at. % *P* doped ZnO films were employed as the channel. Figure 6-1 shows a schematic top view of the field-effect transistor (FET). ZnO-based transparent thin film transistors were fabricated with a top gate electrode. Using prepatterned ITO pads, polycrystalline channel materials were deposited by PLD with the growth temperature of 400°C and the oxygen partial pressure of 20 mTorr and annealed at 600 °C for 1 hr. Thicknesses of channel layer were varied from 20~200nm for FET using undoped ZnO and was set 50nm using 2% P-doped ZnO. The gate oxide of (CeTb)$MgAl_{11}O_{19}$ with 200nm thickness was deposited on undoped ZnO by PLD and HfO_2 with 100nm thickness was grown on 2% P-doped ZnO. The growth temperature was 100°C and room temperature for CTMA and HfO_2, respectively. Al was served for the gate metal. Source and drain patterns were defined by standard photolithography and lift-off techniques. Channel length was 40 μm. Capacitance-voltage (C-V) characteristics were measured at 1MHz using a K590 and current-voltage (I-V) characteristics were performed at room temperature in the atmosphere using KI23 and HP 4145B.

6.3 Results and Discussion

Capacitance-voltage (C-V) characteristics were measured at 1MHz, as shown in figure 6-2 (a). The polarity of the capacitance-voltage characteristic for the device employing nominally undoped ZnO is clearly n-type, with capacitance decreasing with an applied negative voltage. For a MIS diode, the net ionized dopant density, N_A-N_D, can be estimated from the capacitance-voltage behavior, where N_A is the ionized acceptor density and N_D is the donor density. In particular, for a uniformly doped semiconductor, the high frequency capacitance/area in the depletion region is given by

$$N_A - N_D = \frac{2}{q\varepsilon_s}\left[\frac{d}{dV}\left(1/C^2\right)\right]^{-1}$$

where q is the electron charge and ε_s is the permittivity of the semiconductor. From the slope of the plot of $1/C^2$ as a function of V for the diode employing n-type ZnO, the ionized donor density is estimated to be $1.8\text{x}10^{19}/\text{cm}^3$, which is in agreement with Hall measurements for similar polycrystalline ZnO films. The depletion width (W_T) at the depletion-inversion transition point was calculated to be 7.43 nm by

$$W_T = [\frac{2K_s\varepsilon_o}{qN_D}(2\Phi_F)]^{\frac{1}{2}}$$

where K_s is the dielectric constant of ZnO, 8.66, ε_o is the permittivity of free space, q is the electronic charge, N_D is the carrier concentration, and Φ_F is the reference potential related to semiconductor doping concentration. Figure 6-2 (b) shows the hysteresis curve of the C-V plots, indicating that there is little hysteresis effects on the ZnO-based MOS structure. In order to investigate the reliability of MOS diode, I-V characteristics was measured. Figure 6-3 shows the leakage current density of CTMA as a function of applied voltage. The low leakage current of 10^{-6} A/cm^2 was obtained at the applied voltage of 5V.

Figure 6-4 shows the interface trap density of MIS diode between (Ce,Tb)$MgAl_{11}O_x$ and undoped ZnO using Terman method [91]. From the fact that interface traps do not respond to the ac voltage in high frequency C-V measurements, high frequency capacitance can be expressed as $C_{HF} = (C_{ox}C_s)/(C_{ox}+C_s)$ because interface traps respond to the varying dc gate bias. The interface trap density of MIS diode was determined to be $\sim 1\times10^{10}$ eV^{-1} cm^{-2} near the conduction band edge. This Terman method is generally considered to be useful for underestimating interface trap density due to its limitation of insufficient high frequencies.

ZnO-based thin film transistors were fabricated and the thickness of channel materials was varied from 20 to 200nm on patterned substrates of ITO. Figure 6-5 shows the drain current-drain voltage (I_D-V_{DS}) characteristics measured at room temperature for ZnO-based on MOSFET. The modulation of conductance in ZnO indicate that the operation of the device is an n-channel depletion-mode because there were drain currents at the gate voltage of 0V and negative gate voltage was required to reduce the channel conductivity. The small degree of depletion shown in I_D-V_{DS} is caused by a high charge density in the active channel layer as seen in MOS diode. The modulation of conductance of ZnO was more significant in structures with smaller channel thickness due to the difficult generation of depletion regime between source and drain. Figure 6-6 shows the channel conductivity as a function of ZnO layer thickness. With increasing the active channel thickness, the channel conductivity was increased. To make the complete depletion in the channel layer, thinner or low carrier density of active channel layer is desired.

Figure 6-7 shows the capacitance-voltage (C-V) characteristics of $Al/HfO_2/ZnO$ MOS diode measured at 1MHz, indicating that semiconducting oxide has an n-type behavior. No intermediate phase is considered between gate oxide and semiconductor due to the growth of gate oxide at room temperature. Therefore, total capacitance can be written as $1/C_{tot} = 1/C_{ox} + 1/C_{ZnO}$. To determine the flatband voltage, it is assumed that doping distribution in semiconducting layer is uniform. The flatband capacitance was calculated to be 11.2pF and the flatband voltage was 3.19V from the C-V characteristics. The depletion width (W_T) at the depletion-inversion transition point was calculated to be 3.67 nm using Eq. (2).

Figure 6-8 shows the drain current-drain voltage (I_D-V_{DS}) characteristics measured at room temperature for ZnO-based on MOSFET. The gate voltages were varied from –7 to 4V to observe the modulation of conductance, and the drain currents saturate at increasingly higher drain voltage. Modulations of conductance indicate device operates as an n-channel depletion-mode because of the drain current at the gate voltage of 0V and the reduction of drain current with negative gate voltage. The conductivity of 2% phosphorous doped ZnO was 2.5 S cm^{-1} and its value is lower than those of undoped one.

Figure 6-9 shows the drain current (I_D) measured as a function of gate voltage (V_G) at the drain voltage of 10V. The field effect mobility of ZnO-based on MOSFET was 0.192 cm/V s using the transconductance, $\partial I_D/\partial V_G$. The carrier concentration of active channel layer was determined to be $\sim 10^{19}$ cm^{-3}. The leakage current of gate oxide in n-channel device was on the order of $\sim 10^{-5}$A at the gate voltage of 2V.

The small degree of I_{on}/I_{off} ratio is caused by a high charge density in the active channel layer. In depletion-mode device, the modulation of conductance is more significant in structures with smaller channel thickness due to the generation of depletion regime through semiconducting layer. To make the complete depletion in the channel layer, it will be interesting to further investigate thinner or low carrier density of active channel layer.

6.4 Conclusions

We have fabricated ZnO based-transparent thin film transistor (TFT) structures on glass using pulsed laser deposition. Capacitance-voltage properties are measured after formation of metal-oxide-semiconductor (MOS) structures, indicating that undoped and phosphorous-doped ZnO is n-type semiconducting material with little hysteresis when the gate voltage is swept. Interface trap density between gate oxide, CTMA, and undoped ZnO is determined to be $\sim 1\times10^{10}$ eV^{-1} cm^{-2} near the conduction band edge. Undoped and phosphorous-doped ZnO-based TFTs show the depletion-mode device operation from drain current-drain voltage measurements.

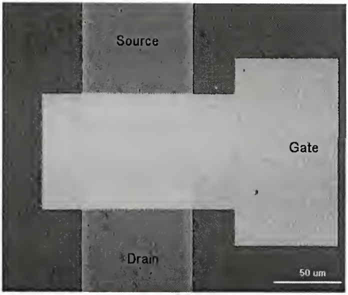


Figure 6-1. Schematic top view of the ZnO-based thin film field-effect transistor

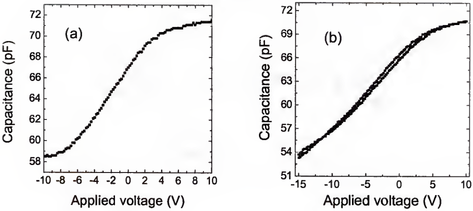


Figure 6-2. C-V characteristics of MOS diode using undoped ZnO as a semiconducting layer with electrode area of 3.14×10^{-4} cm^2

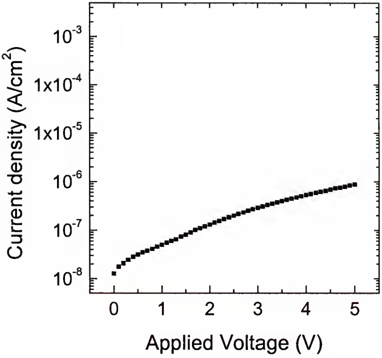


Figure 6-3. I-V characteristics of MOS diode using undoped ZnO as a semiconducting layer with electrode area of 3.14×10^{-4} cm^2

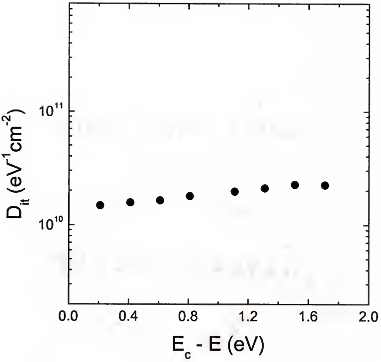


Figure 6-4. Interface trap density of MOS diode between (Ce,Tb)$MgAl_{11}O_x$ and undoped ZnO using Terman method

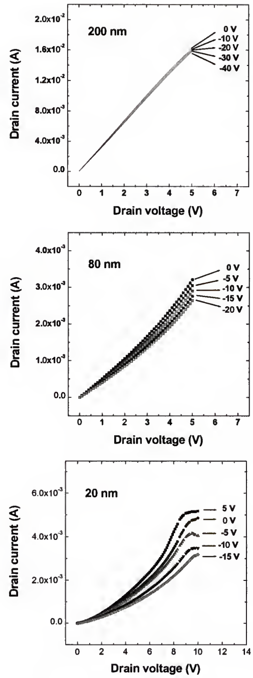


Figure 6-5. I_D-V_{DS} characteristics of ZnO-based on TFT with different thickness of active channel layer from 20 to 200nm

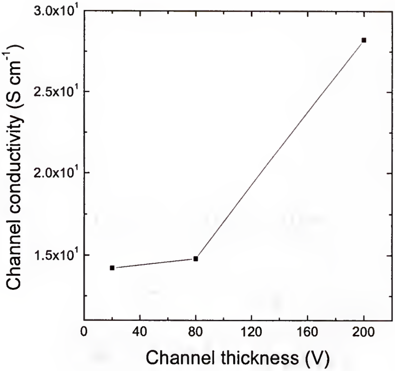


Figure 6-6. Channel conductivity of undoped ZnO as a function of channel thickness in the thin film field-effect transistors

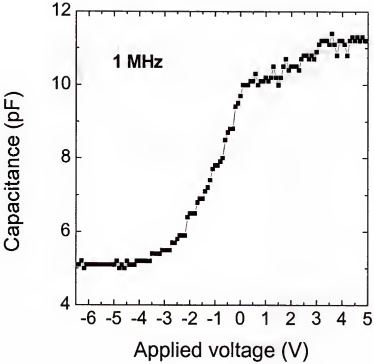


Figure 6-7. C-V characteristics of TFT using 2% phosphorus-doped ZnO as an active channel layer

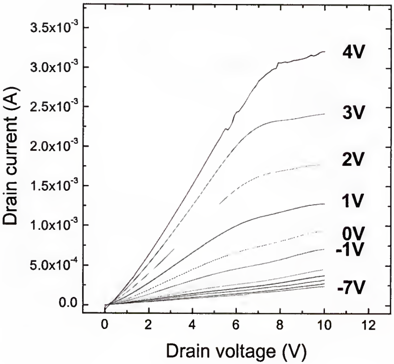


Figure 6-8. I_D-V_{DS} characteristics of TFT using 2% phosphorus-doped ZnO as an active channel layer

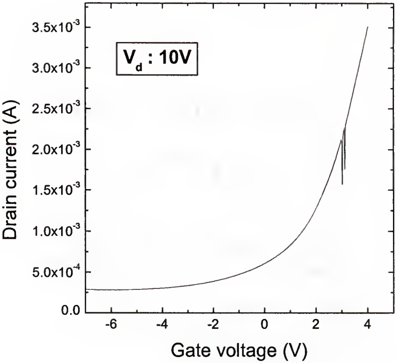


Figure 6-9. Transfer characteristics of TFT using 2% phosphorus-doped ZnO as an active channel layer

CHAPTER 7

ENHANCEMENT MODE THIN-FILM FIELD-EFFECT TRANSISTOR USING PHOSPHOROUS-DOPED (ZN,MG)O CHANNEL

7.1 Introduction

Thin films of transparent conducting oxides (TCOs) have been widely investigated as electrode materials in various applications, such as light-emitting displays, semiconductor devices, and solar cells [98-104]. The prerequisites of TCOs are a wide optical band gap (>3 eV), high electrical conductivity, and optical transmittance (>80%) in the visible region [105]. As wide band-gap semiconductors, TCOs are also attractive as the active materials in transparent electric and optoelectrics technologies. Transparent field-effect transistors (FETs) have been explored using other wide band-gap semiconductors, including GaN [106] and SiC [107]. However, wide gap semiconducting oxides appear to be more attractive for transparent transistor development as they can be synthesized as thin films at lower temperatures that are compatible with various substrates, including glass. Among the semiconducting oxides, ZnO is particularly attractive in terms of low-temperature synthesis and semiconducting properties. ZnO is an *n*-type II–VI compound semiconductor with a direct band gap of 3.35 eV. The crystal structure of ZnO is hexagonal (wurtzite) with $a = 3.25$ Å and $c = 5.12$ Å. Electron doping via defects originates from Zn interstitials in the ZnO lattice [108]. *n*-type doping is caused by the intrinsic defect levels approximately 0.05 eV below the conduction band. The Hall mobility of ZnO single crystals at room temperature is on the order of 200 $cm^2 V^{-1} s^{-1}$ [109]. Semiconducting ZnO films can be deposited at a temperature ranging from

300–700 °C using various deposition techniques. Hall mobility for polycrystalline films ranges from 10–50 $cm^2\ V^{-1}\ s^{-1}$. Furthermore, *p*-type ZnO was recently reported by molecular-beam epitaxy [110], radio-frequency (rf) sputtering [111], and hybrid beam deposition [112]. Based on these characteristics, transparent FETs (TFETs) using ZnO as an active channel layer are being explored [37-39,113,114].

One of the major challenges in ZnO-based FET development is to control the carrier density in the active channel. As-deposited ZnO films tend to display a high carrier density, even for materials that are nominally undoped. A high carrier density yields a channel that will be conducting in the absence of applied gate voltage. Device functionality occurs via depletion of carriers with applied field. Hence, this is a depletion mode device. High channel carrier densities prove difficult to deplete. More preferable is an enhancement mode device, in which conductivity is induced via applied gate voltage. In this article, the properties of thin-film FETs that utilize *P*-doped $Zn_{0.9}Mg_{0.1}O$ as the active channel materials are reported. Recently, it has been shown that phosphorus substitution introduces an acceptor level that reduces the electron density or, in some case, yields *p*-type behavior. A further reduction in carrier density can be achieved via Mg doping. In this case, Mg substitution increases the band gap, thus increasing the activation energy for defect-related donor states. The use of *P* and/or Mg doping yields an opportunity to tailor the channel conductance for enhancement mode operation. When doping to control channel conductance, one issue that must be addressed is the impact that phosphorus and/or Mg doping has on the channel mobility.

7.2 Experiments

The substrates used for these devices were indium-tin-oxide (ITO)-coated glass. Prepatterned ITO pads serve as the source and drain regions. $Zn_{0.9}Mg_{0.1}O$ films doped with 2 at. % *P* were employed as the channel. HfO_2 was selected as the gate dielectric as it exhibits a large band gap sufficient to yield a positive band offset with respect to ZnO. The top gate electrode was sputter-deposited Al. Figure 7-1 shows a schematic cross section and top view of the FET using 2% *P*-doped $Zn_{0.9}Mg_{0.1}O_{0.98}$ as an active channel layer. The transistors were fabricated in a top gate electrode geometry. Using patterned ITO-coated glass as the substrate, the polycrystalline channel layer was deposited by pulsed laser deposition. The growth temperature was 400 °C with an oxygen partial pressure of 20 mTorr. For unannealed $Zn_{0.9}Mg_{0.1}O{:}P_{0.02}$ grown at 400 °C, Hall measurements yield a mobility on the order of 2–3 $cm^2/V\ s$ with a carrier density of 3–$5\times10^{19}/cm^3$. After the channel material was formed, it was annealed at 600 °C in 20 mTorr oxygen partial pressure for 1 h. This is necessary to activate the phosphorus dopant, yielding high resistivity ZnO. Hall measurements on annealed films yield resistivity greater than 400 Ωcm. This temperature is lower than that needed to yield a similar decrease in carrier density in undoped ZnO films. Thickness of the semiconducting channel layer was 50 nm. A HfO_2 film was deposited on the channel layer by rf magnetron sputtering with a gate oxide thickness of 100 nm. The gate oxide film was amorphous when deposited at room temperature in the oxygen partial pressure of 5 mTorr. Al with 100 nm thickness was deposited for the gate metal by magnetron sputtering. The source and drain regions were then exposed by standard photolithography and selective wet etching. Channel length and channel width were 20 μm and 90 μm, respectively. Capacitance–voltage (*C*–*V*) characteristics were measured at 1 MHz. Current–voltage (*I*–*V*) characteristics were performed at room temperature using an Agilent 4155A Semiconductor Parameter Analyzer.

7.3 Results and Discussion

The *C–V* characteristics of the gate metal Al/HfO_2/ZnO structure was measured at 1 MHz. The polarity of the accumulation capacitance indicates that semiconducting oxide is *n*-type behavior, although doping with an acceptor reduces the carrier density considerably. We assume there is no intermediate reaction layer between the gate oxide and ZnO semiconductor, as the gate oxide was deposited at room temperature. If the doping density is uniform throughout the semiconducting layer, the flatband voltage is given by

$$C_{FB} = \frac{1}{(d/\varepsilon_{ox}) + (L_d/\varepsilon_s)}$$

where d is the thickness of gate oxide, $L_d = (\varepsilon_{ZnO}\varepsilon_0 kT/q^2 N_D)^{1/2}$ is the Debye length of the *n*-type ZnO, k is the Boltzmann constant, T is the absolute temperature, q is the magnitude of the electron charge, ε_{ox} and ε_s are the permittivity of HfO_2 and ZnO, respectively, and N_D is the electron concentration. The flat-band capacitance was calculated to be 3.76 pF and the flatband voltage was 3.78 V from the *C–V* characteristics. Some degree of hysteresis was observed in the *C–V* measurement for devices employing HfO_2 as the gate oxide film, indicating the presence of mobile ions in the HfO_2 film.

Figure 7-2 shows the drain current–drain voltage (I_D–V_{DS}) characteristics measured at room temperature for ZnO based on a metal–oxide semiconductor FET. The modulation of the $Zn_{0.9}Mg_{0.1}O$:P channel conductance indicates that the operation of the device is an *n*-channel enhancement mode, as there is little drain current at a gate voltage of 0 V. Note that the leakage current is relatively high through the HfO_2 gate dielectric, yielding a nonzero intercept of *I–V* curves taken at finite gate voltage. This high gate current limited the ultimate gate voltage that could be applied, with this limiting the on/off ratio that can be realized. Further improvement in the gate dielectric will improve performance. Current saturation and pinch off are clearly observed, indicating that the entire channel region can be depleted of electrons. These characteristics are useful for circuit applications that employ these devices.

Drain current (I_D) and gate current (I_G) were measured as a function of gate voltage (V_G) at a fixed drain voltage of 6 V. These results are shown in Figure 7-3. The field-effect mobility can be determined from the transconductance using

$$I_D = \frac{W}{L}\mu_{FE}C_{ox}(V_{GS} - V_T)V_{DS}$$

where W is the channel width, L is the channel length, C_{ox} is the capacitance of gate oxide, V_T is the threshold voltage, and μ_{FE} is the field-effect mobility. The extracted field-effect mobility is 5.32 $\mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$. This value is comparable to that realized in undoped ZnO channels, and indicates that acceptor doping did not have a detrimental impact on channel mobility. This may reflect the likelihood that mobility in the polycrystalline channel is determined by the grain-boundary scattering which is present in the doped and undoped case. The threshold voltage for this device is 2.8 V. The carrier concentration in the channel is estimated to be $3.9\times10^{16}\ \mathrm{cm}^{-3}$. The channel conductivity is $3.3\times10^{-2}\ \mathrm{S\ cm}^{-1}$ at the gate voltage of 0 V. The on/off current ratio is on the order of $\sim10^3$ at the gate voltage of 10 V at a drain voltage of 6 V. The zero bias off current was $\sim10^{-7}$ A. Gate leakage current at a bias of 4 V was 1.2×10^{-6} A.

Figure 7-4 shows the conductance of channel materials, undoped ZnO, 2% phosphorous-doped ZnO, and 2% phosphorous-doped $\mathrm{Zn_{0.9}Mg_{0.1}O}$. The results indicate that the use of P doping yields lower channel conductance than undoped ZnO, and Mg doping to *P*-doped ZnO make a further reduction in carrier density. By using these characteristics, an enhancement-mode transistor is realized.

7.4 Conclusions

We report on enhancement-mode ZnO-based field-effect transistors that utilize an acceptor-doped channel. In particular, the active channel is polycrystalline ZnO doped with Mg, to increase the band gap, and *P*, to decrease the electron carrier concentration. Devices are realized that display an on/off ratio of 10^3 and a channel mobility on the order of 5 cm^2/V s. HfO_2 serves as the gate dielectric. Capacitance–voltage properties measured across the gate indicate that the ZnO channel is *n* type. The use of acceptor doping improves the control of the initial channel conductance while having a minimal impact on channel mobility relative to undoped ZnO polycrystalline channels.

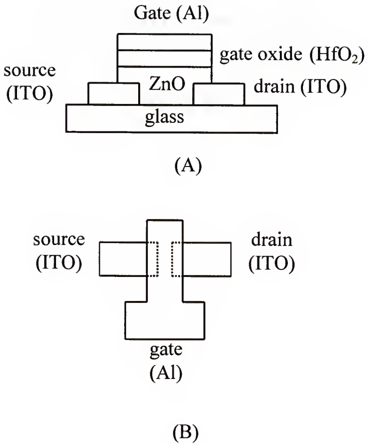


Figure 7-1 Schematic (A) cross-sectional and (B) top view of the ZnO-based thin-film transistor

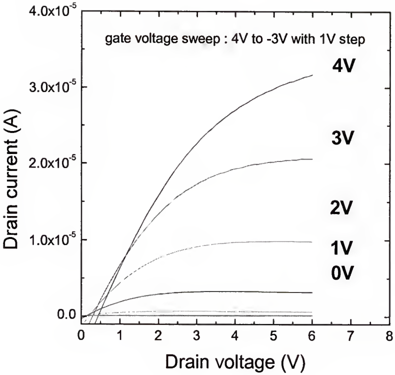


Figure 7-2. I_D–V_{DS} characteristics of ZnO-based TFT with channel length of 20 μm and channel width of 90 μm

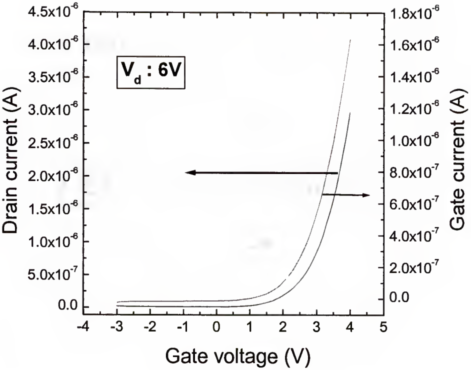


Figure 7-3. Transfer characteristics of ZnO-based TFT measured at drain voltage of 6 V

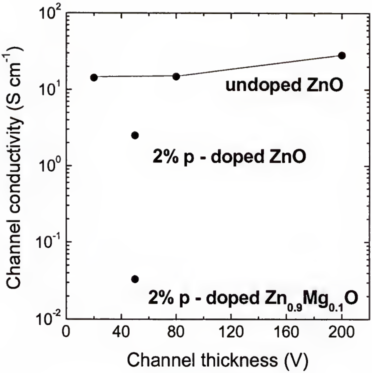


Figure 7-4. Conductivity of different channel materials

CHAPTER 8
SUMMARY

The crystallinity of $CaHfO_x$ on various substrates was investigated. $CaHfO_x$ on Si had high crystallization temperature, 800°C, and its phase was polycrystalline. Using Ge substrate, the crystallinity of $CaHfO_x$ indicated that (101) planes were developed at 850°C and showed the polycrystalline phases with (101) and (121) planes. In the case of the growth of $CaHfO_3$ films on biaxially textured Ni, (101) plane was well developed more than (121) plane at high temperature. $CaHfO_3$ film on $LaAlO_3$ seemed to be heteroeitaxy developed with $CaHfO_x(101)$ // $LaAlO_3(100)$.

The stability of amorphous calcium hafnate thin films was also compared with related zirconate. The X-ray diffraction results showed that amorphous hafnates film was thermally stable up to 850°C more than amorphous zirconate film. The dielectric constant for $CaHfO_x$ was determined to be 13 and the interfacial layer of SiO_2 between $CaHfO_x$ film and Si substrate had 8.6Å thickness from C-V characteristics. The flatband capacitance and voltage was extracted from the C-V measurement and the fixed charge density was estimated to be $7.49 \times 10^{11}/cm^2$. The hysteretic behavior from C-V measurements and a relatively high leakage current from I-V characteristics were observed.

The electrical properties of an amorphous ultra-wide band gap aluminate have been demonstrated. The leakage current density for $Ce_{0.33}Tb_{0.67}MgAl_{11}O_x$ films with MIM structure was very low, measured at room temperature to be $\sim 10^{-6} A/cm^2$ at an applied field of 5MV/cm. The conduction mechanism was studied using ITO substrate and determined to be Schottky emission. The interface trap densities of amorphous aluminate were ~1×10^{12} eV^{-1} cm^{-2} and ~3×10^{12} eV^{-1} cm^{-2} from Terman and conductance method, respectively.

Depletion mode field-effect transistors were achieved with undoped ZnO and 2% phosphorous doped ZnO for an active channel layer. The conductivity of undoped ZnO was observed as a function of channel thickness, indicating that the channel conductivity was increased with increasing the active channel thickness. Undoped and doped ZnO showed n-type behavior from C-V measurement. Due to its high carrier concentrations, the small degree of I_{on}/I_{off} ratio was obtained.

Enhancement mode field-effect transistor was realized with 2% phosphorous doped (Zn,Mg)O for an active channel layer. Well-saturated drain current versus drain voltage curve was obtained. The field-effect mobility was 5.32 cm^2 V^{-1} s^{-1}, the carrier concentration in the channel is estimated to be 3.9×10^{16} cm^{-3}, and the channel conductivity is 3.3×10^{-2} S cm^{-1}.

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BIOGRAPHICAL SKETCH

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He established the Gator Kendo Club, with other members at the University of Florida, in 2000. Yongwook actively participated in the club and instructed club members. The UF Kendo club won 1st place in the team matches. Yongwook was the winner in the individual matches at the Florida championship, 1st Annual Tournament of the Cherry Blossoms, held in 2003.

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